(In)GaAs MOS and MOSFETs

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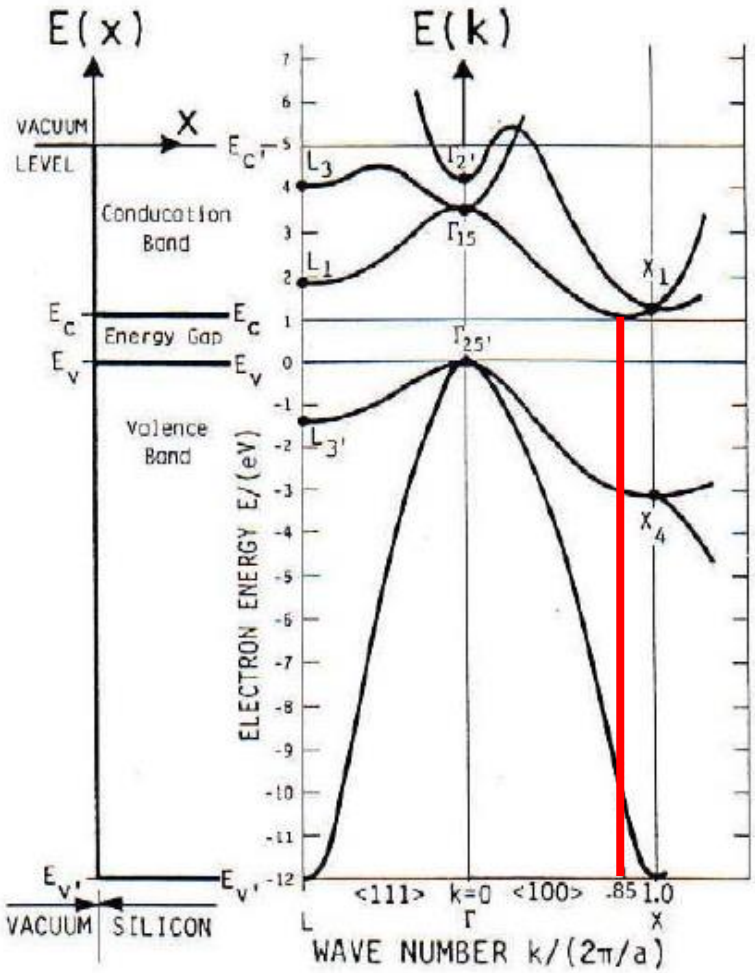
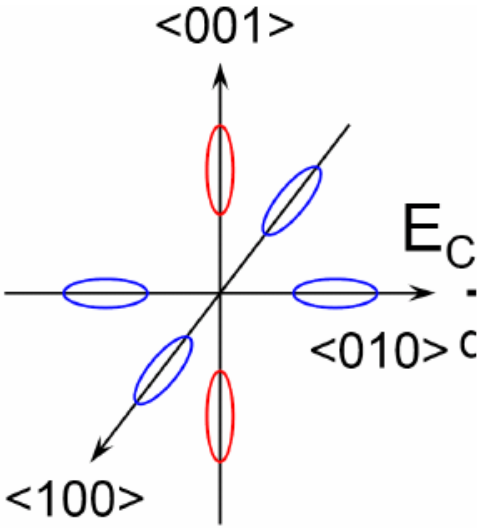
Outline

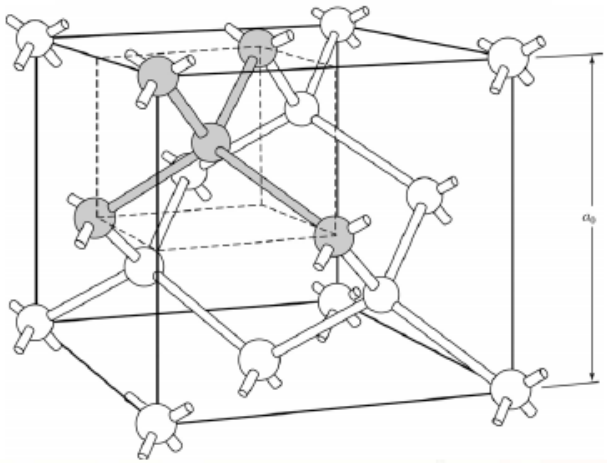
- Introduction
  - Metal-oxide-semiconductor (MOS) structure
  - MOS capacitor analysis
  - MOS field-effect transistors (MOSFETs)
- High dielectric constant (κ) oxides on (In)GaAs
  - High carrier mobility materials
  - High-κ oxides
  - *In-situ* preparation of oxide/semiconductor interfaces
- High-κ on (In)GaAs MOSCAPs and MOSFETs
  - MBE-HfO_2, Y_2O_3 and ALD-Y_2O_3 on GaAs MOSCAPs
  - ALD-HfO_2 and Al_2O_3 on $In_{0.53}Ga_{0.47}As$ MOSFETs
  - Common gate MBE-Y_2O_3 for Ge, GaSb and $In_{0.53}Ga_{0.47}As$ MOSCAPs and MOSFETs

Semiconductor band structure

Si band structure

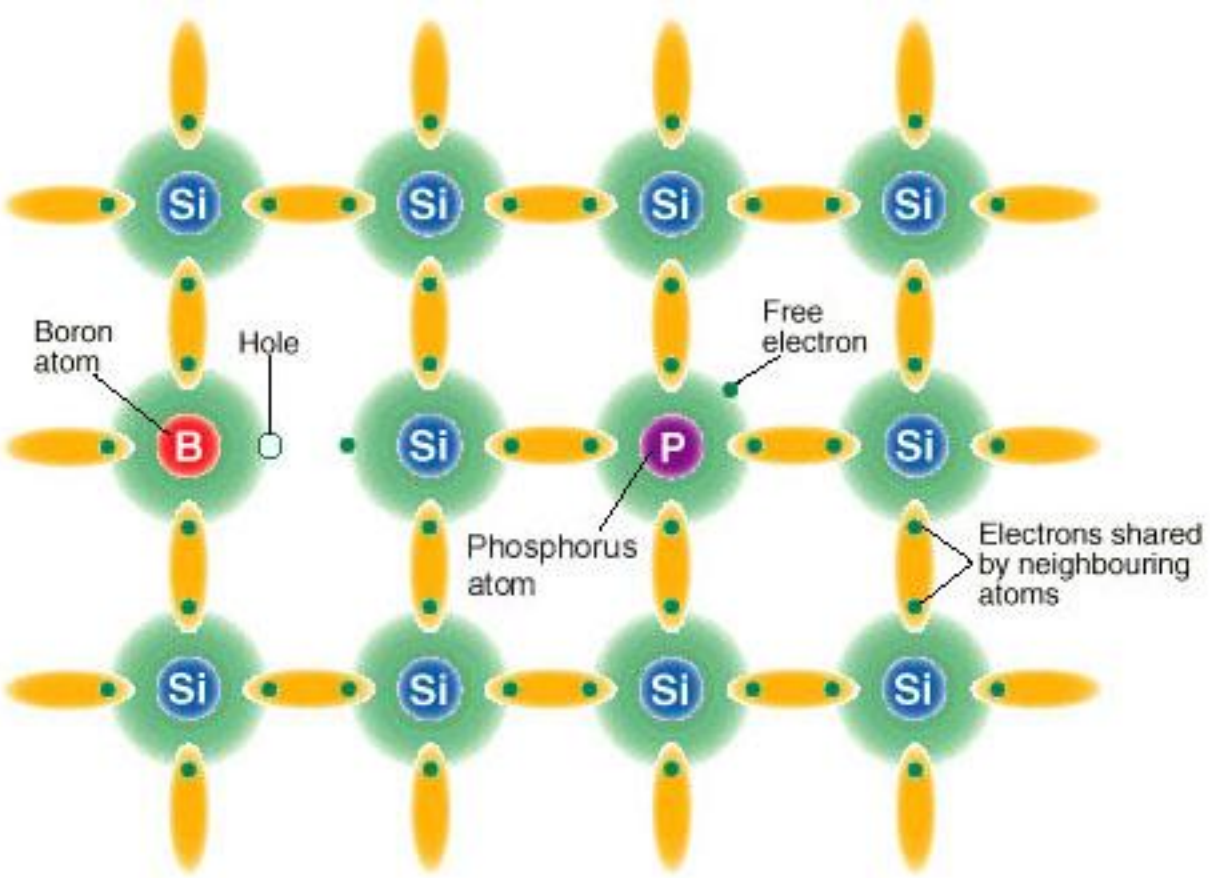






Doping in semiconductor

Doped Si: Boron (p-type), Phosphorous (n-type)

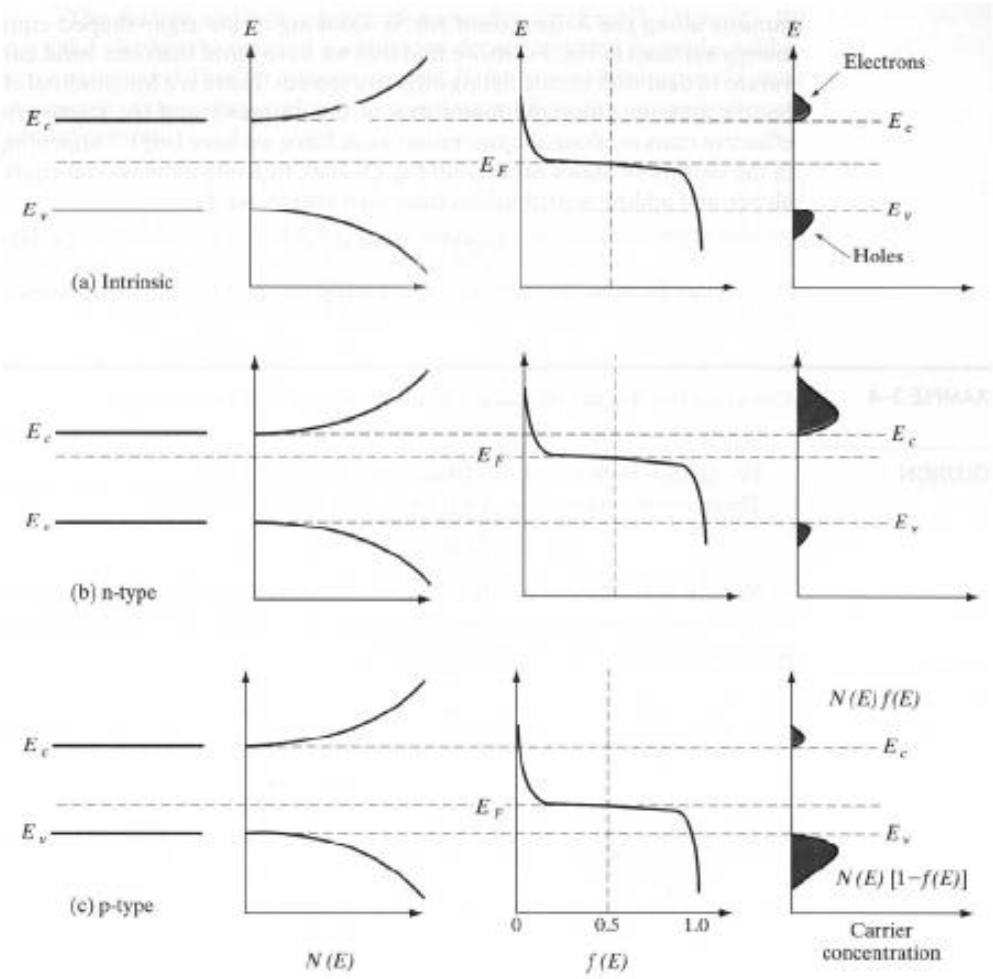


Fermi level in semiconductor

Intrinsic

n-type

p-type



n ∼ p

n >> p

n << p

carrier conc.

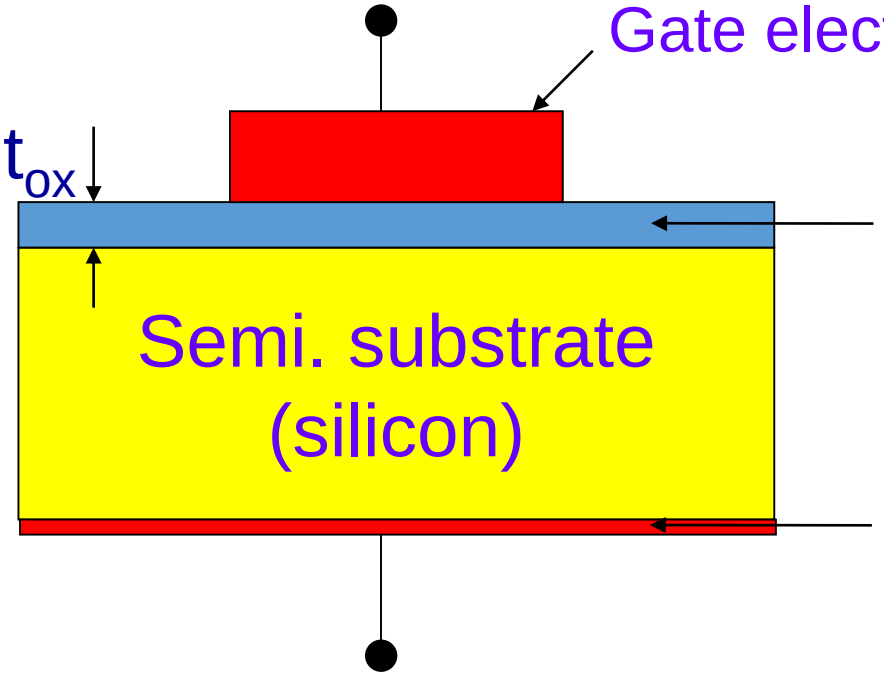
Mathematically

$$n = \int_{E_c}^{E_c'} f(E)D(E)dE \qquad (6)$$

$$p = \int_{E_v'}^{E_v} [1 - f(E)]D(E)dE \qquad (7)$$

Metal-oxide-semiconductor structure

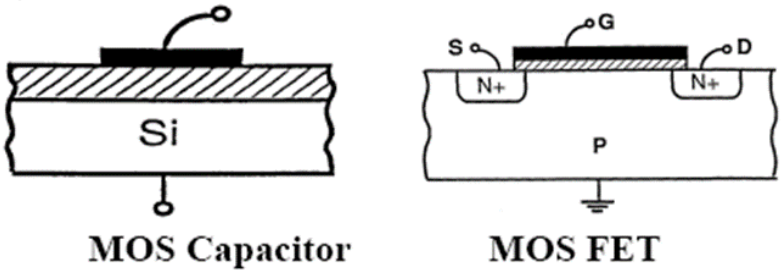
MOS structure (capacitor/diode) :



$C = \varepsilon_0 \varepsilon_i A/t_{ox}$

Advantages

- MOSFET-like structure
- Easy fabrication
- Interfacial information acquired prior to device (MOSFET) processing



Operation principle of MOS capacitor

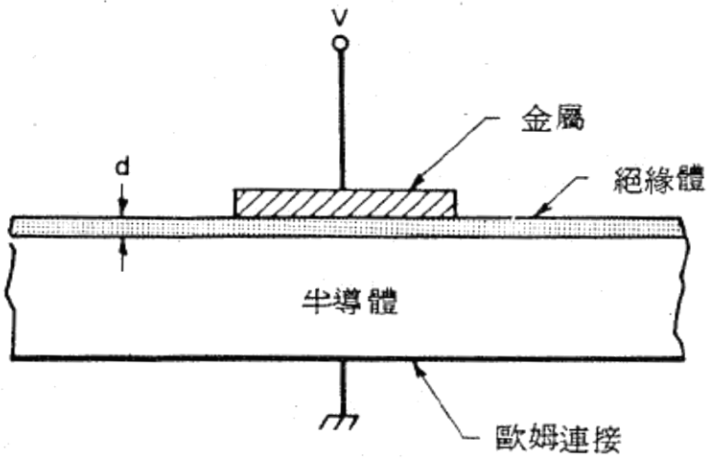
Fermi level alignment when $V_G = 0$ (equilibrium)

Flat band condition (ideal) :

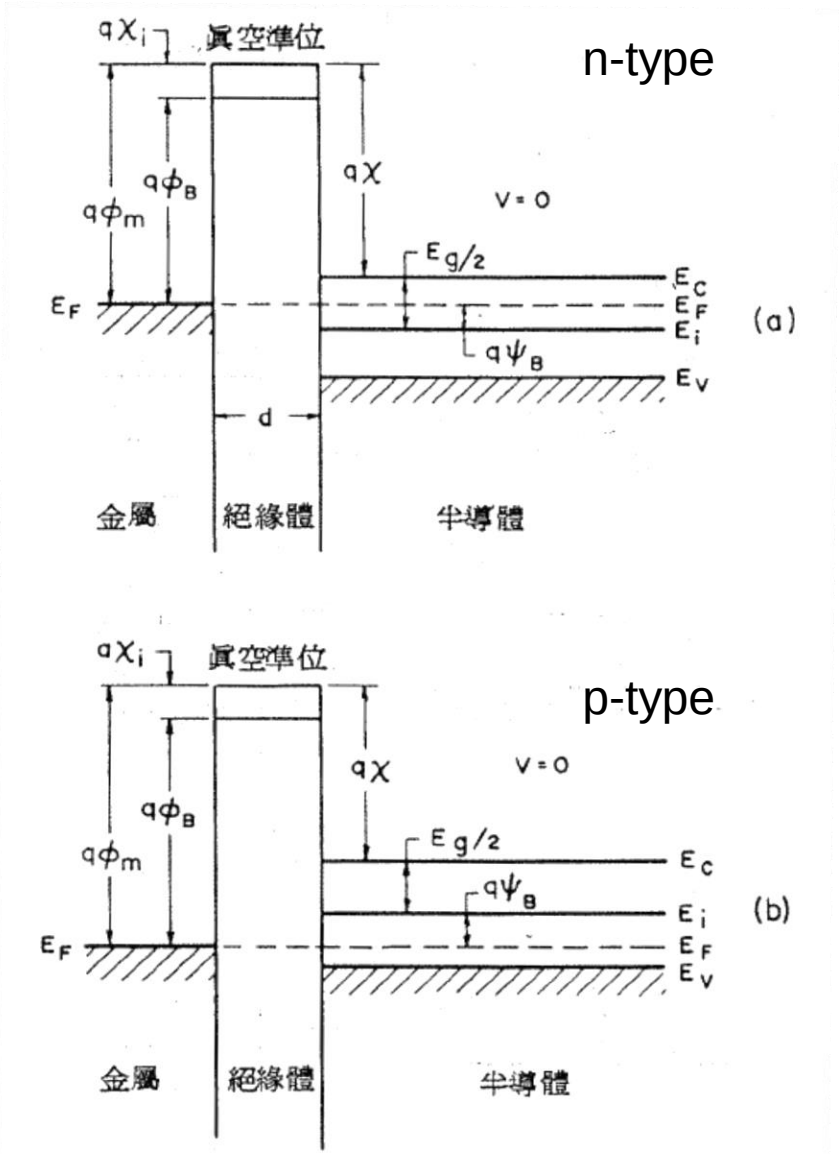
$V_G = V_{FB} = 0$ *when* $\phi_{ms} = 0$

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B\right) = 0 \qquad \text{for } n\text{-型}$$

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_B\right) = 0 \qquad \text{for } p\text{-型}$$



金屬 - 絕緣體 - 半導體（MIS）二極體的結構

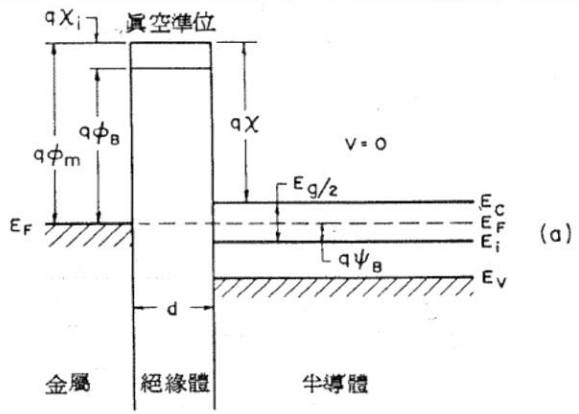


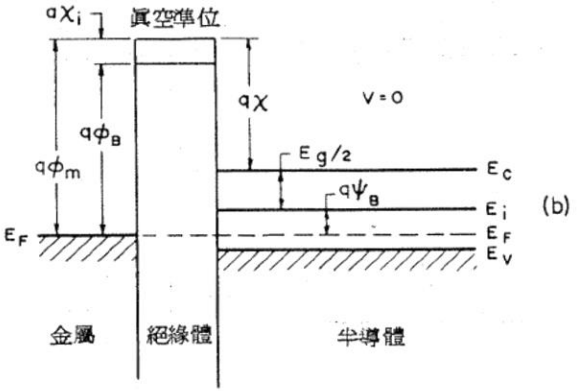
電壓$V=0$時，理想的MIS二極體之能帶圖形。(a)為 n 型半導體；(b)為 p 型半導體

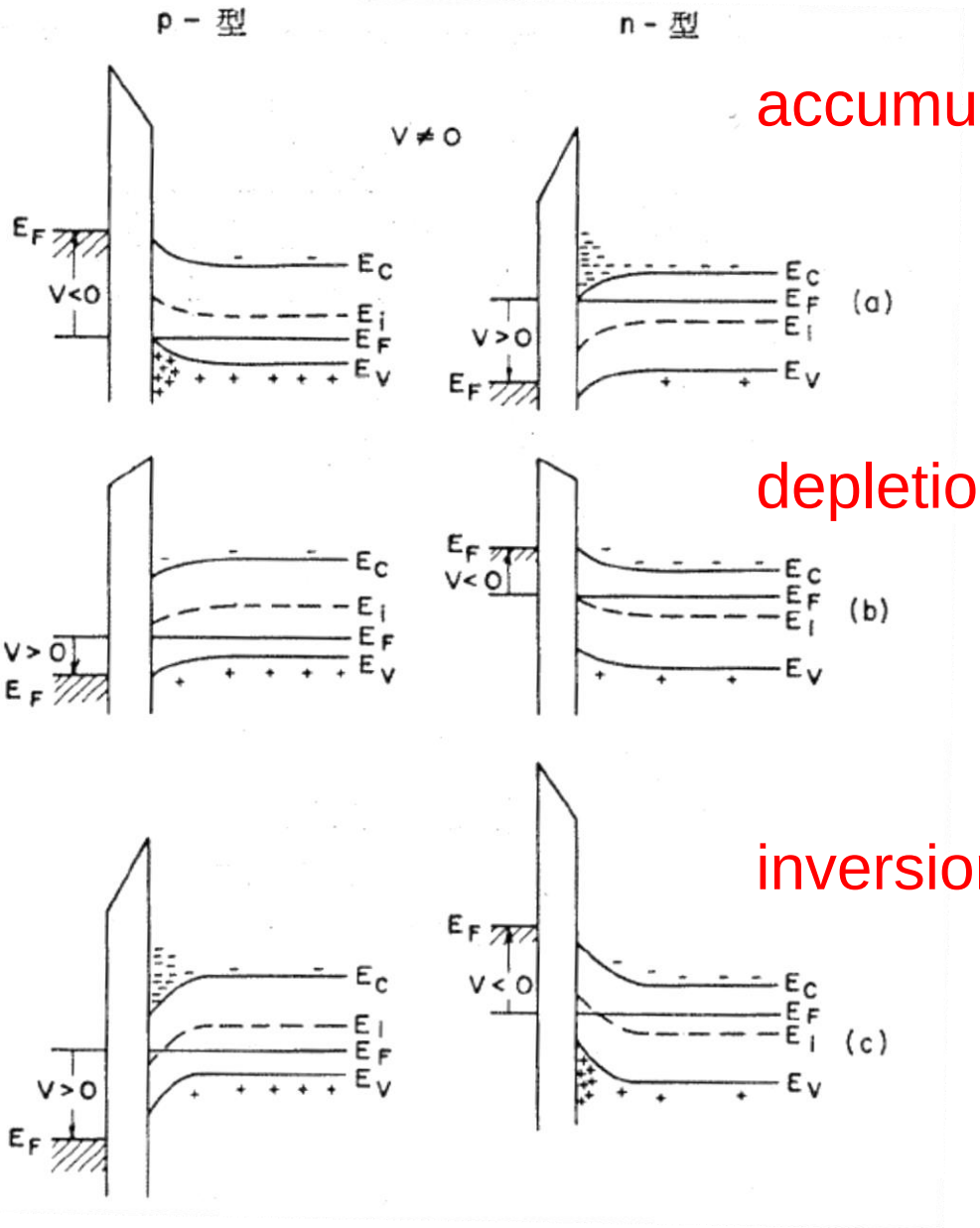
Operation principle of MOS capacitor

Flat band condition (ideal) :

$V_G = V_{FB} = 0$

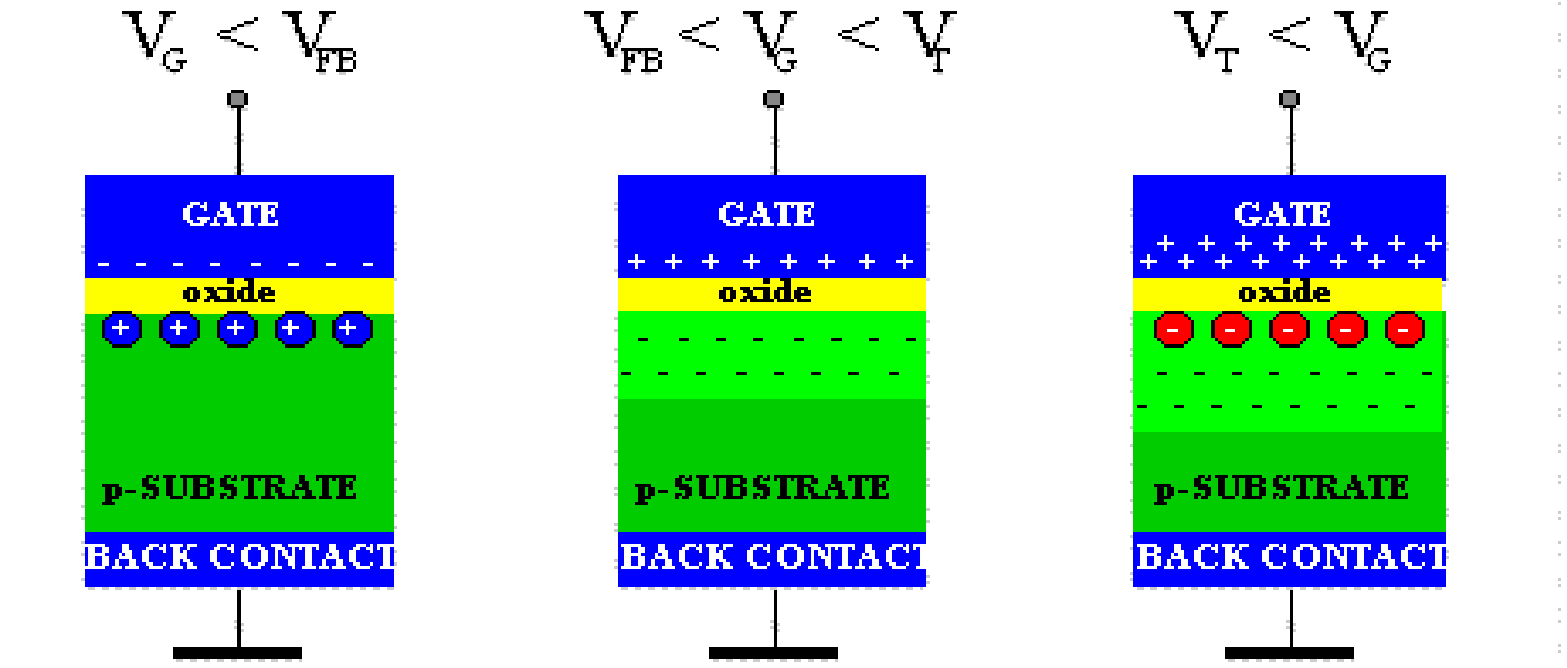






Operation principle of MOS capacitor

Schematics of an MOS capacitor under different bias modes



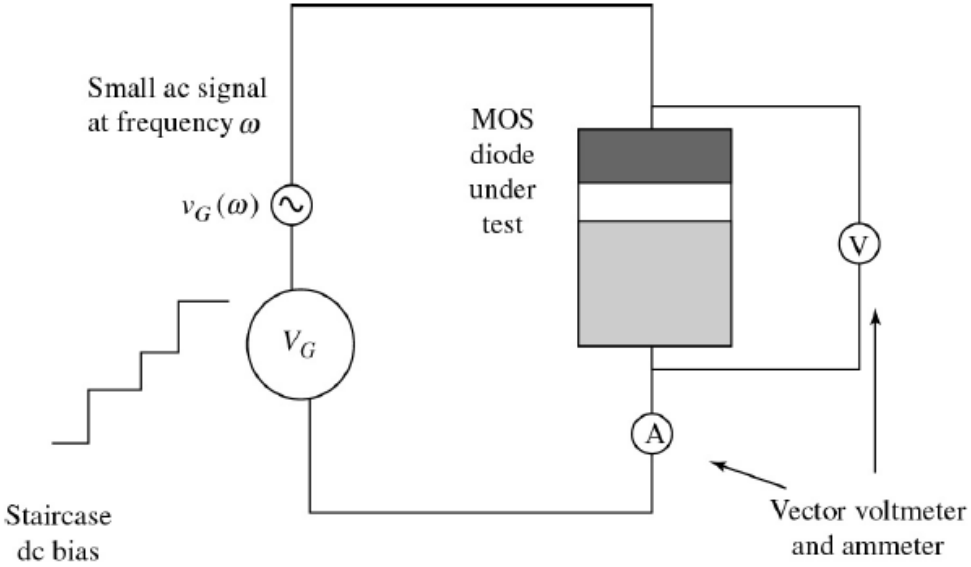
accumulation of majority carriers

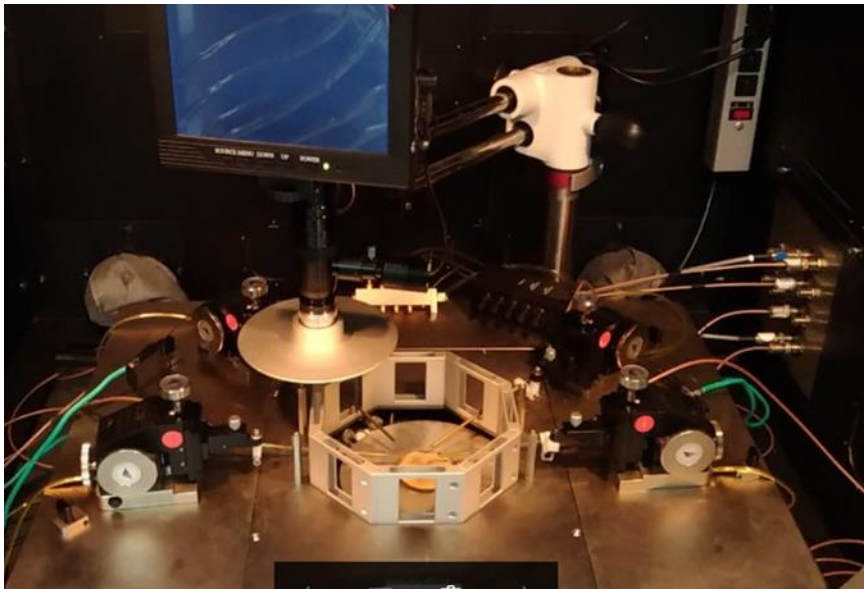
depletion of majority carriers

accumulation of minority carriers

MOS capacitor analysis

MOS *capacitance-voltage (C-V)* measurement :





small amplitude ac signal (100 Hz to 1 MHz) on staircase dc bias

differential capacitance :

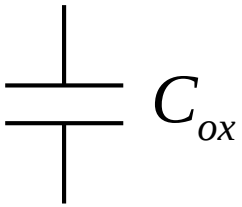
$$C = \frac{\Delta q}{\Delta V}$$

at some voltage V

MOS capacitor analysis

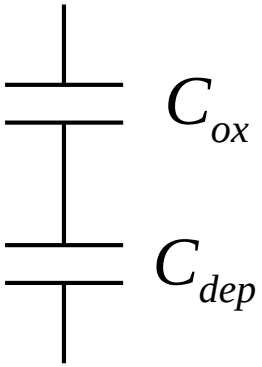
MOS small-signal capacitance model :

Accumulation



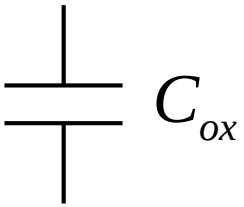
incremental charge located at semiconductor surface

Depletion

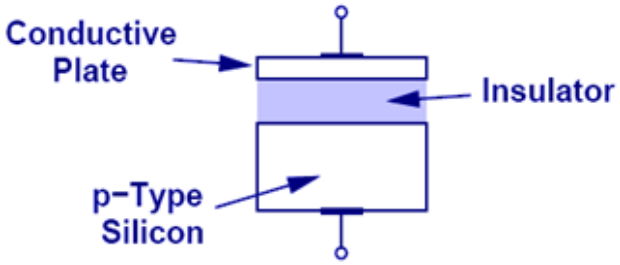


Incremental charge located at bottom edge of depletion region

Inversion



Incremental charge located at semiconductor surface



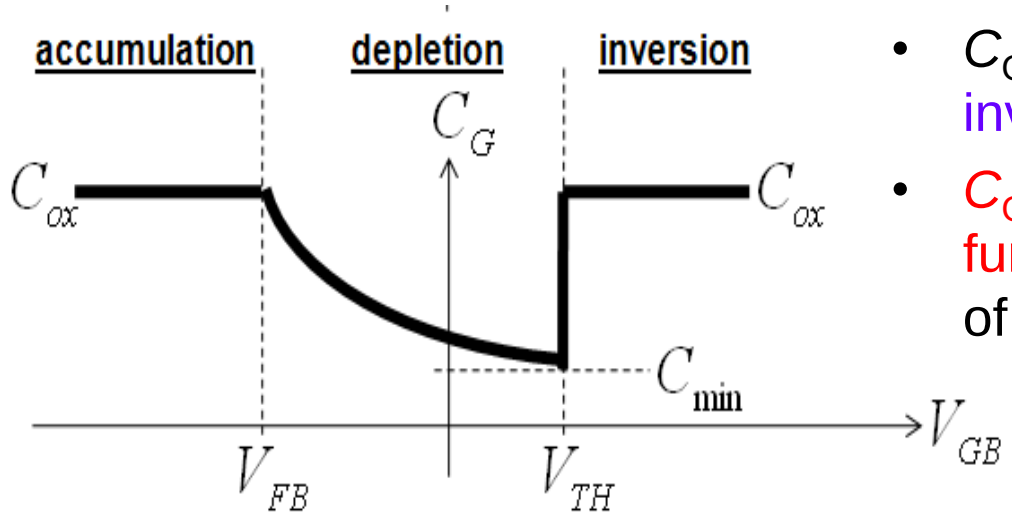
$$C_{ox} \equiv \frac{\varepsilon_{ox}}{t_{ox}}$$

oxide capacitance

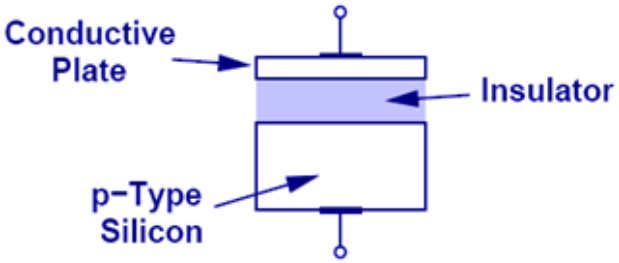
$$C_{dep} \equiv \frac{\varepsilon_{Si}}{X_d}$$

MOS capacitor analysis

MOS *capacitance-voltage (C-V)* curve :



- $C_G = C_{ox}$ in the accumulation and inversion regions of operation.
- C_G is smaller, and is a non-linear function of V_{GB} in the depletion region of operation.

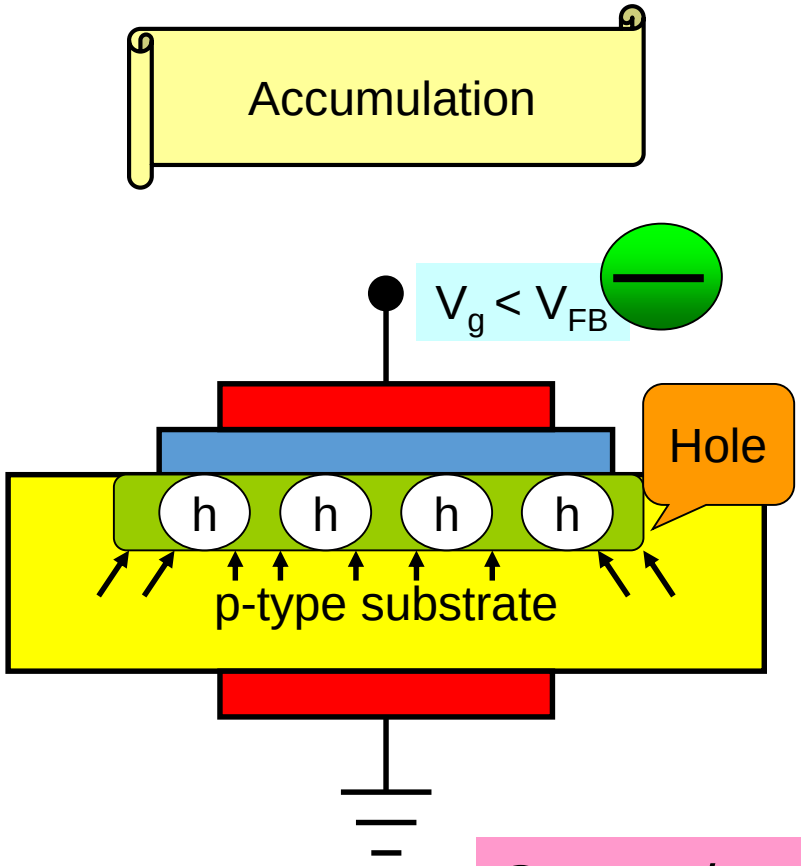


$$C_{\min} = \frac{C_{ox} C_{dep,\min}}{C_{ox} + C_{dep,\min}}$$

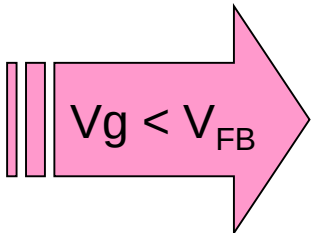
where $C_{dep,\min} \equiv \frac{\varepsilon_{Si}}{X_{d,\max}}$

MOS capacitor analysis

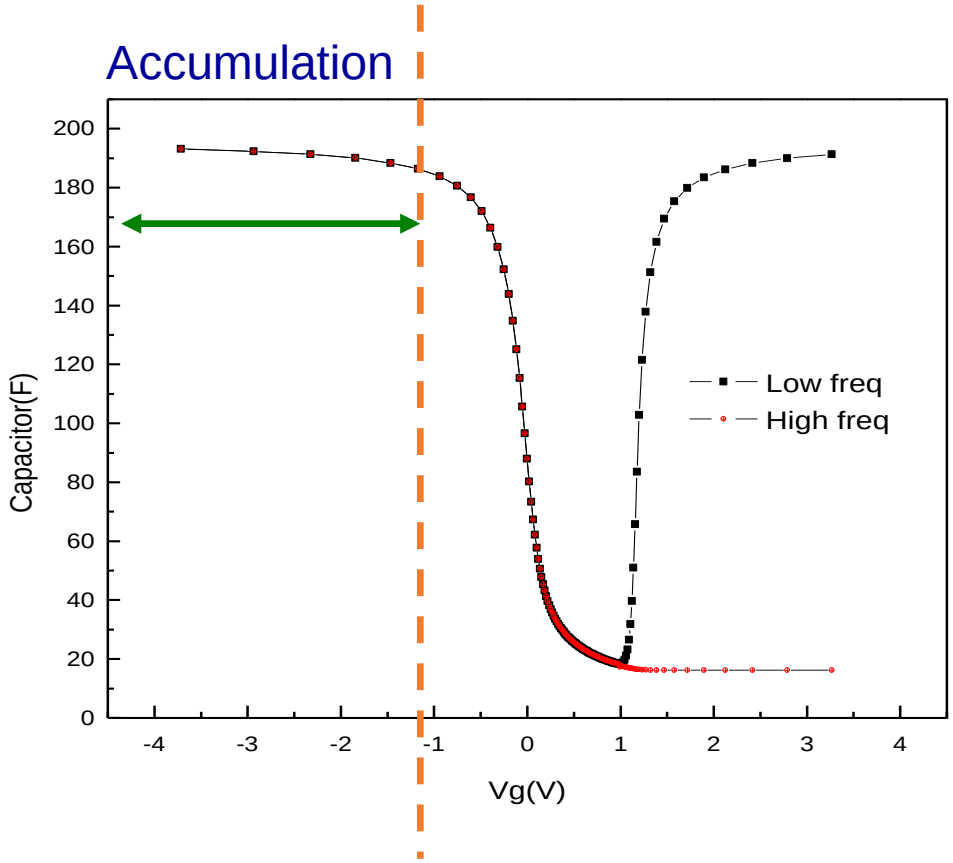
MOS *capacitance-voltage (C-V)* curve :



$C_{ox}=\varepsilon_{ox}/t_{ox}$



Simulation of *C-V* curve



MOS capacitor analysis

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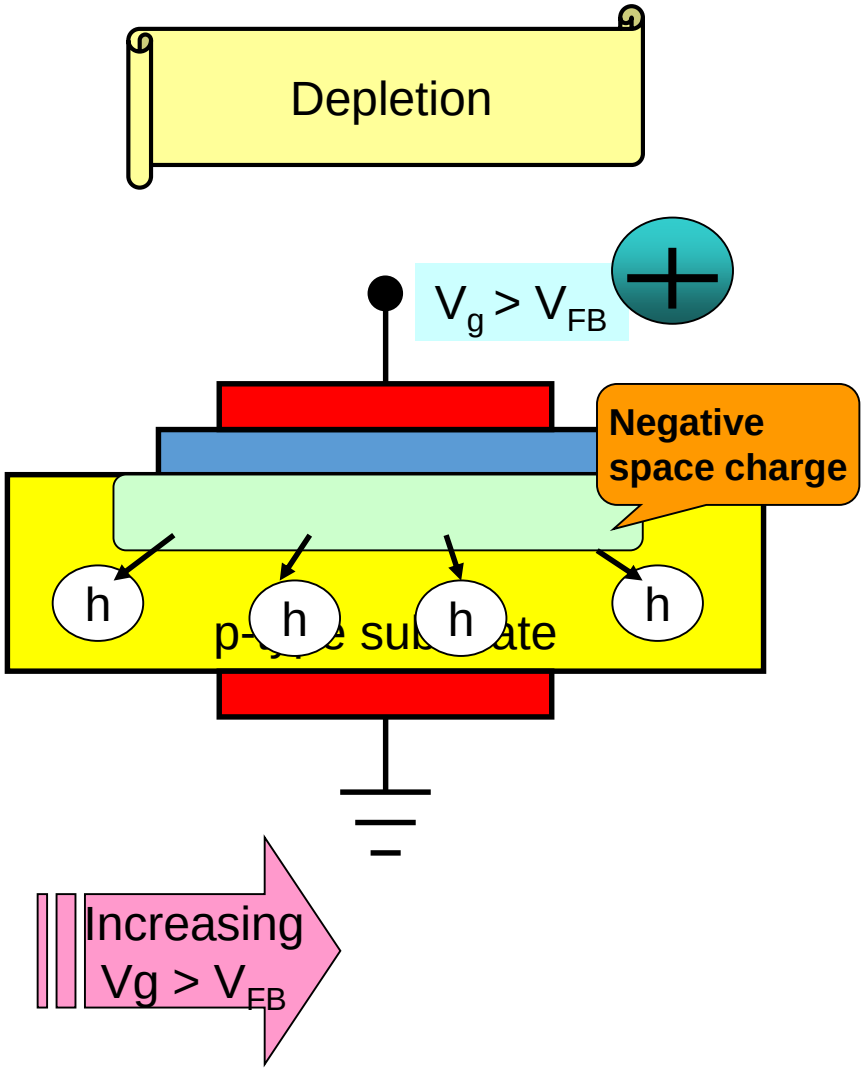

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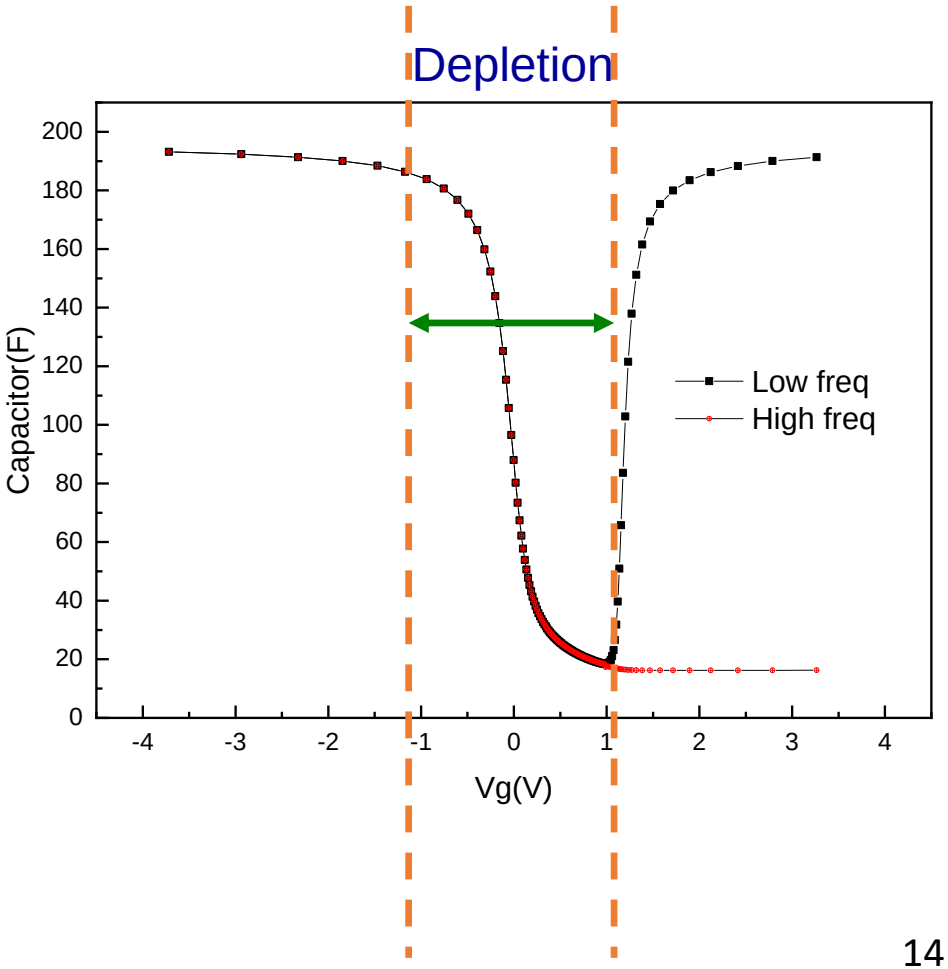

MOS capacitor analysis

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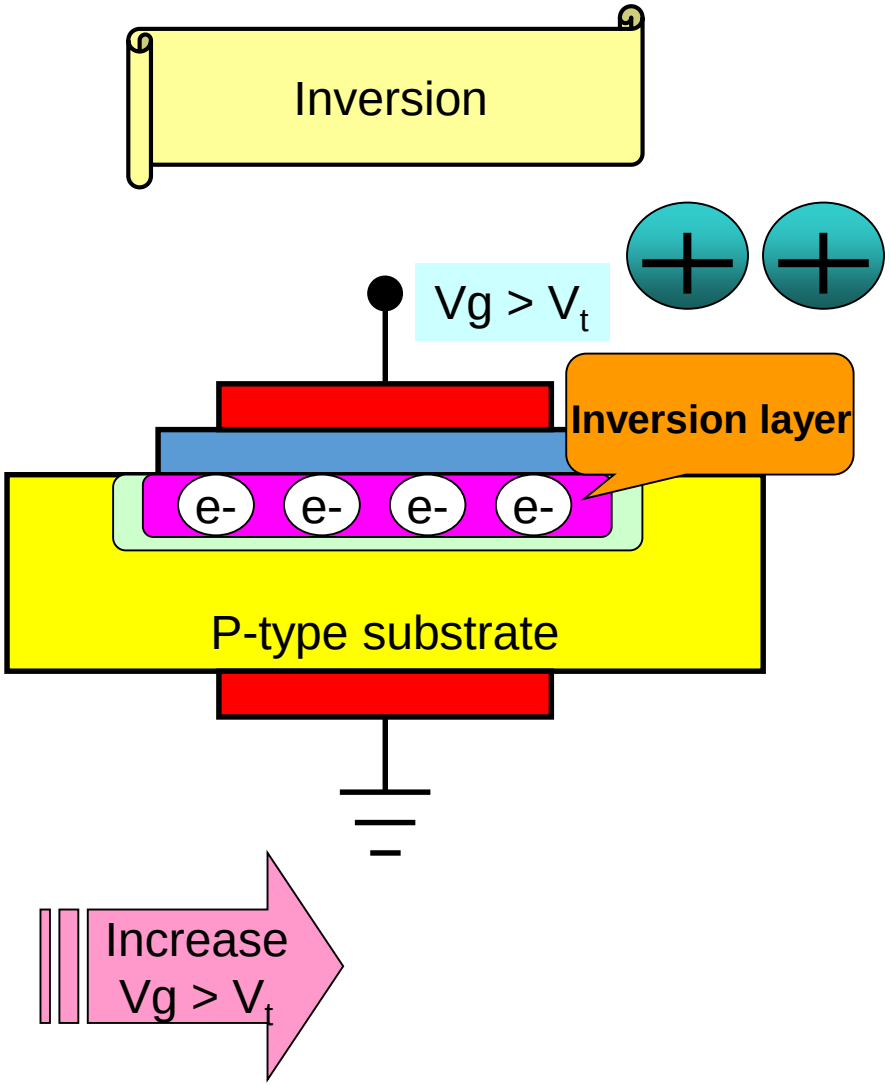
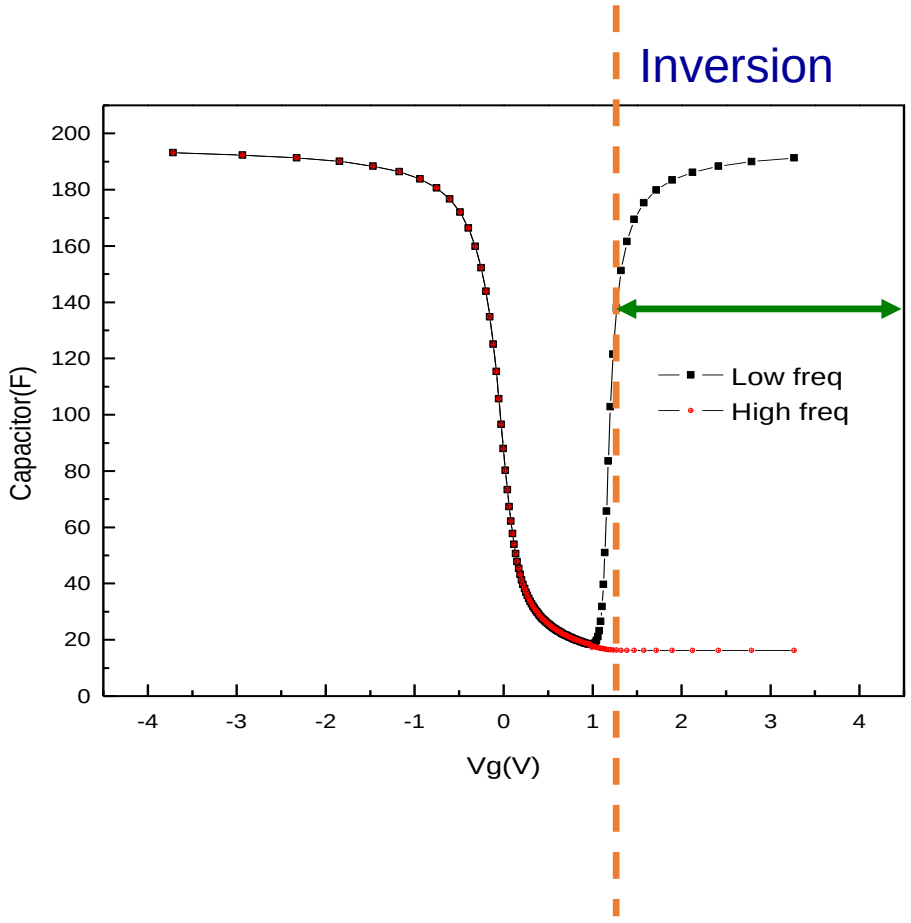


Simulation of *C-V* curve



MOS capacitor analysis

Frequency dependence :

- **Low frequency**

  Charge equilibrium maintains at all times. The capacitance is the ratio of the change in charge to the change in gate voltage, measured while the capacitor is in equilibrium.

  low frequency- dV_g is slow enough to change Q_{inv}

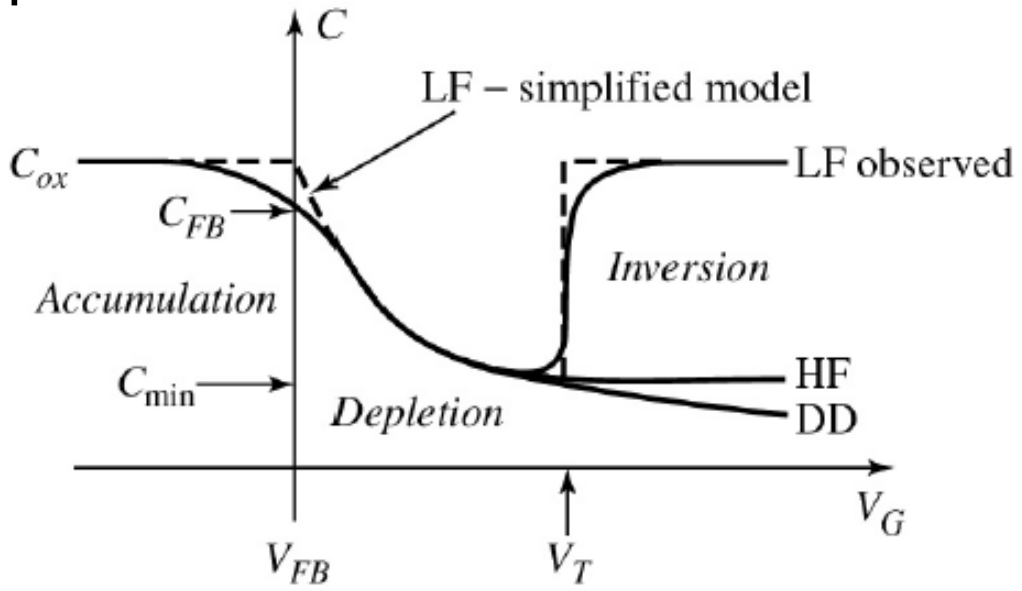
- **High frequency**

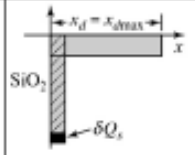
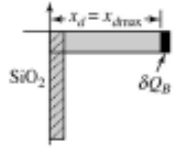
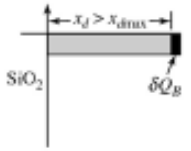
  Under this condition, one finds that the charge in the inversion layer does not change from the equilibrium value at the applied dc voltage. The high frequency capacitance therefore reflects only the charge variation in the depletion layer and the (rather small) movement of the inversion layer charge.

  high frequency- dV_g is too fast to change Q_{inv}

MOS capacitor analysis

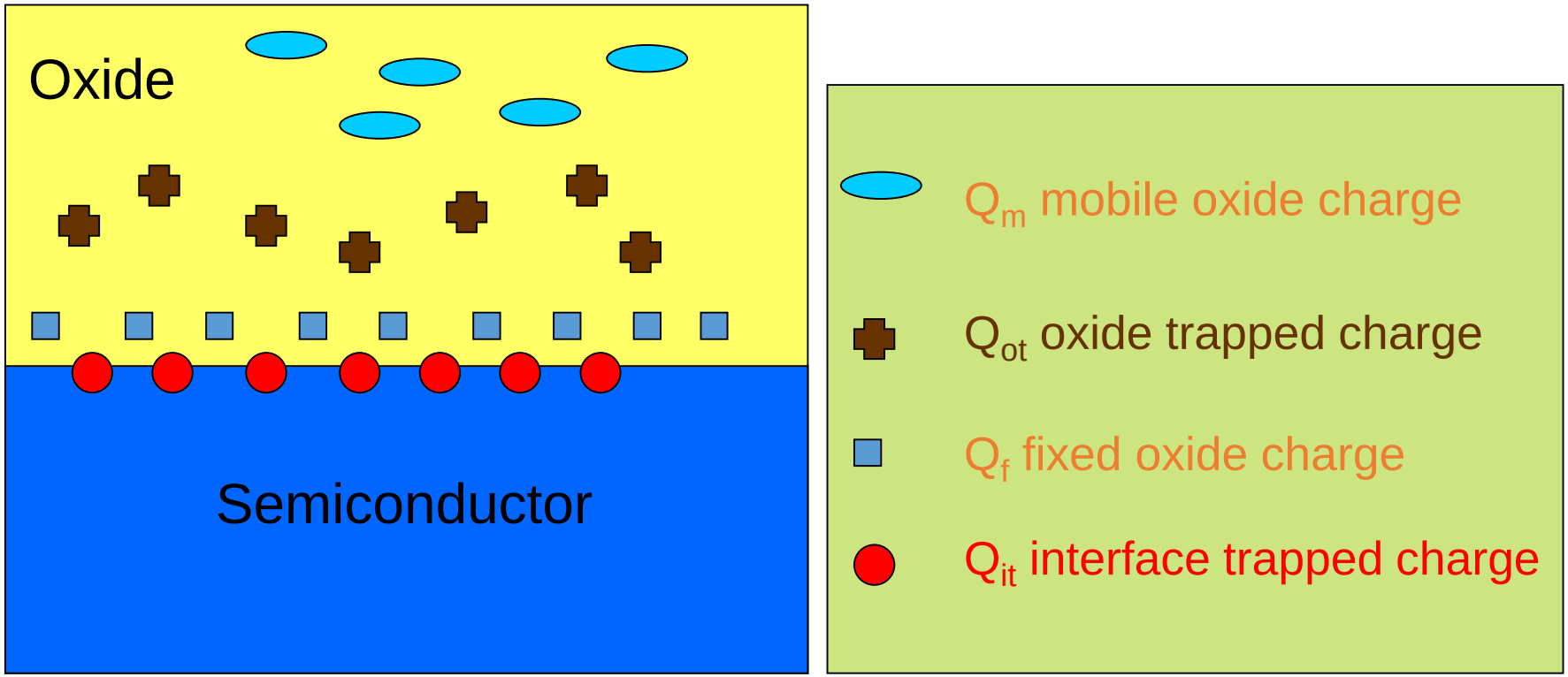
Frequency dependence :



Bias Condition	Charge Equilibrium	Charge Distribution	Equivalent Circuit	Comment
Low frequency (LF)	dc equilibrium ac equilibrium			$\delta Q_s = \delta Q_n$ ac coupling only to surface charge
High frequency (HF)	dc equilibrium ac nonequilibrium			$\delta Q_s = \delta Q_d$ ac coupling only to bulk charge
Deep depletion (DD)	dc nonequilibrium ac nonequilibrium			both ac and dc coupling to Q_d $x_d > x_{dmax}$

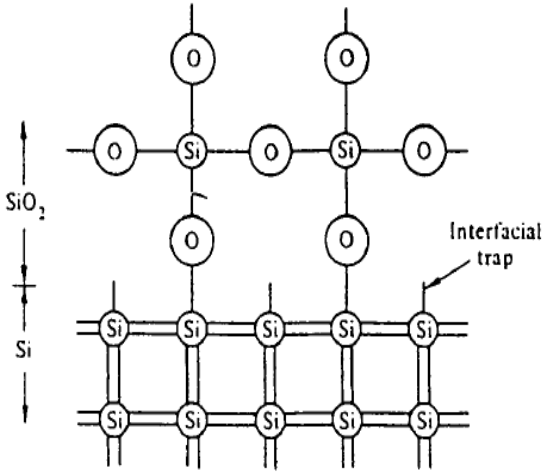
Non-ideal effects in MOS capacitor

Charges in oxide layer :

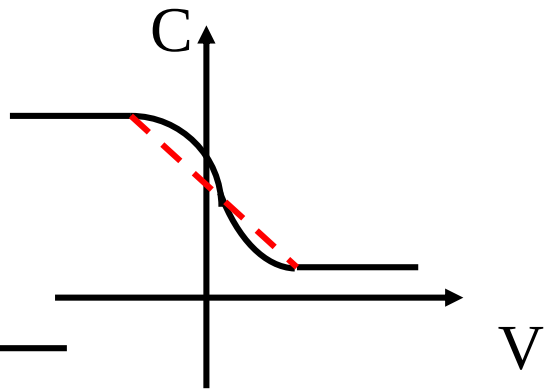


Non-ideal effects in MOS capacitor

Interface trapped charge Qit :



Interfacial traps
(Si dangling bonds)



$D_{it} = 0$

D_{it} is not 0

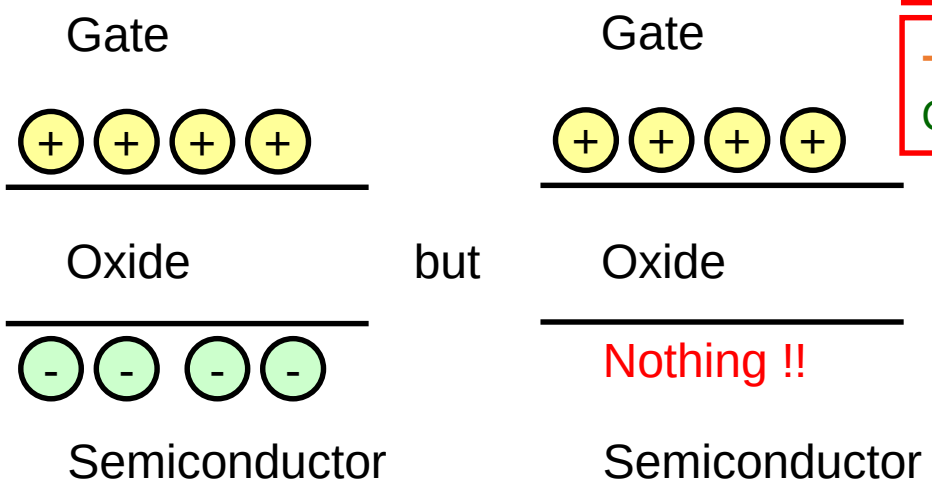
For the same Vg, the surface potential with D_{it} is smaller.

The *C-V* curve is lengthened.

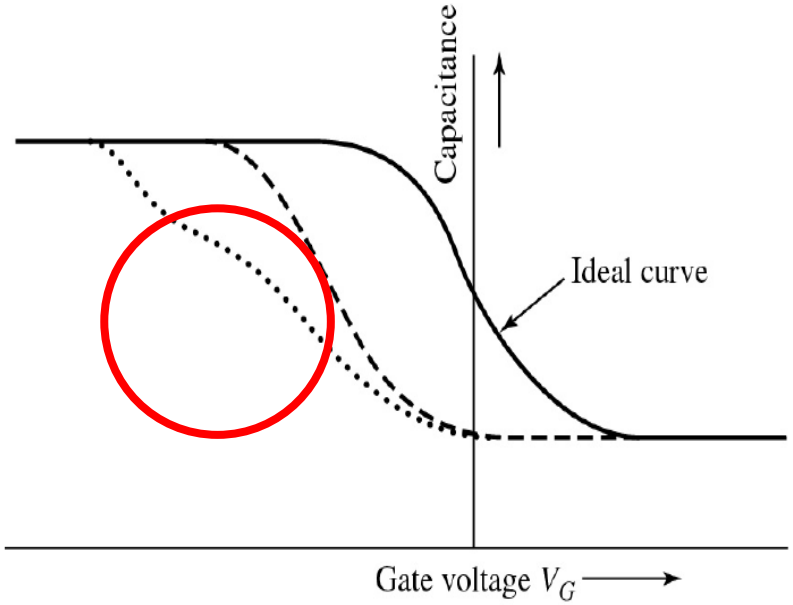
Non-ideal effects in MOS capacitor

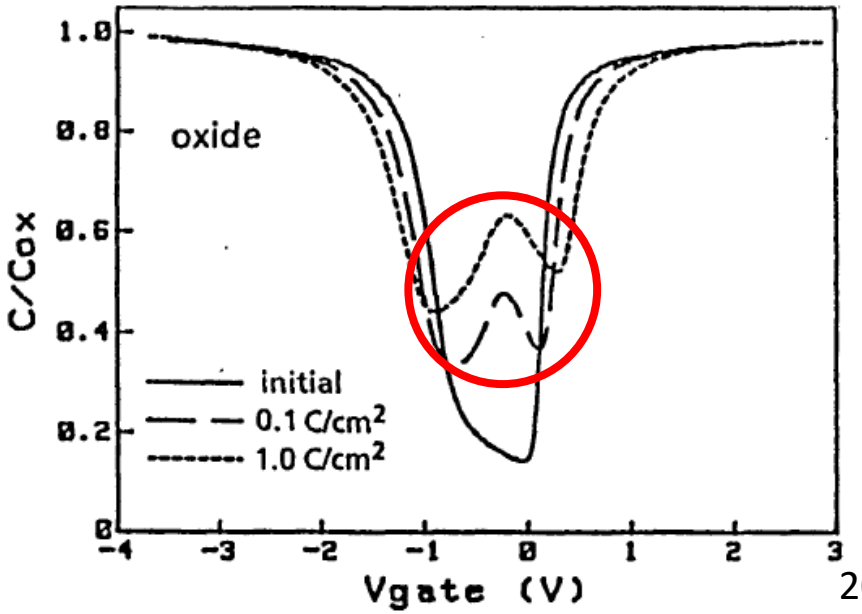
Interface trapped charge Qit :

- **Distortion in C_{HF}-V curve**
  Interface charges Q_{it} varied with V_{gb}
- **Peaks in C_{LF}-V curve**
  C_{trap} from charging-discharging

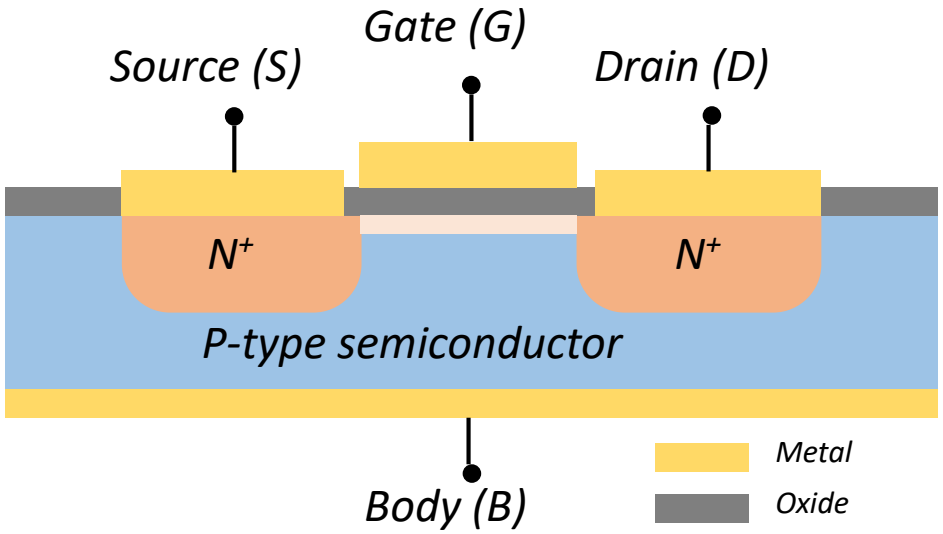


Interface traps



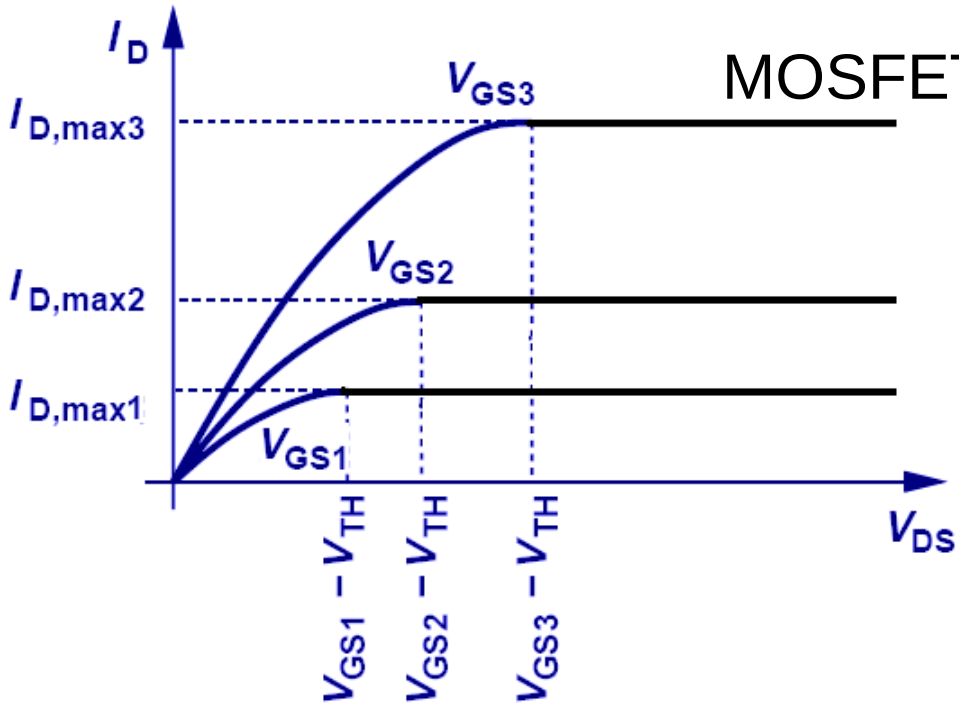


MOS field-effect transistor



self-aligned process

- **gate patterning**
- **S/D imp./activ.**
- **S/D contact metal**
- **Pad metal**



MOSFET I_D-V_G $\frac{I_{D,sat}}{W} \propto \frac{\kappa\varepsilon_0}{t_{ox}} \frac{\mu}{L_G}(V_G - V_T)^2$

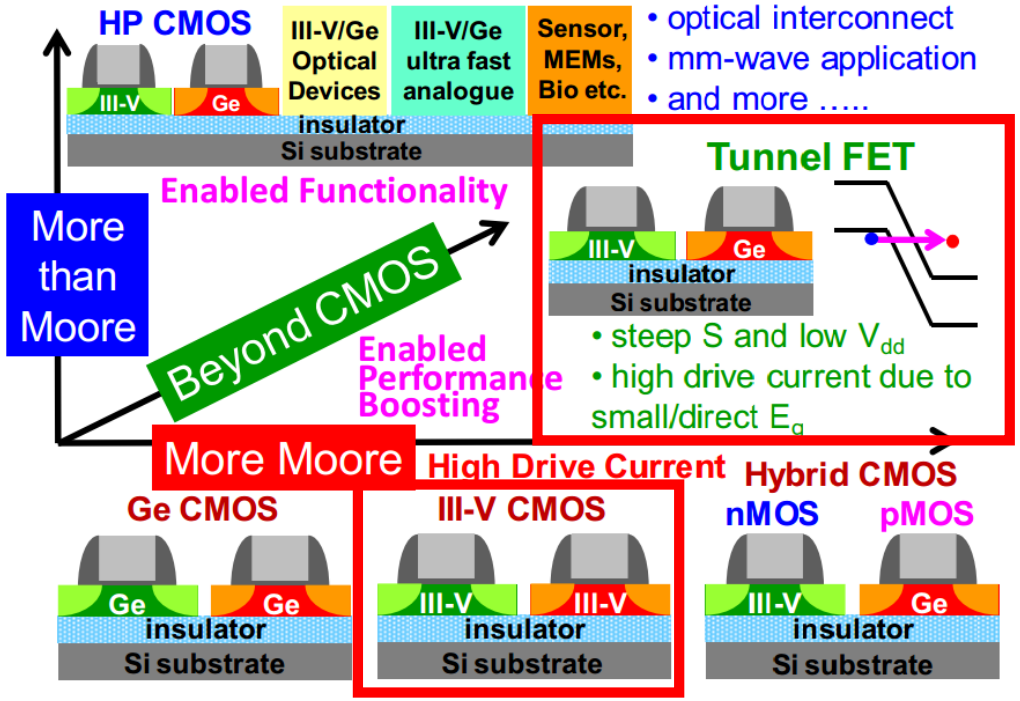
- ✓ Dimensional scaling
- ✓ High-mobility semiconductors
- ✓ High-κ dielectrics

But, the most important issue is the interface quality!

High carrier mobility materials

Property \ Material	IV		III-V				
	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	GaSb	InSb
Electron Mobility ($cm^2/V{\cdot}s$)	1,400	3,900	8,500	12,000	40,000	3000	77,000
Hole mobility ($cm^2/V{\cdot}s$)	450	1,900	400	450	500	1000	1250
Bandgap (eV)	1.11	0.67	1.42	0.74	0.36	0.72	0.17

- **High-speed and low-power logic devices**

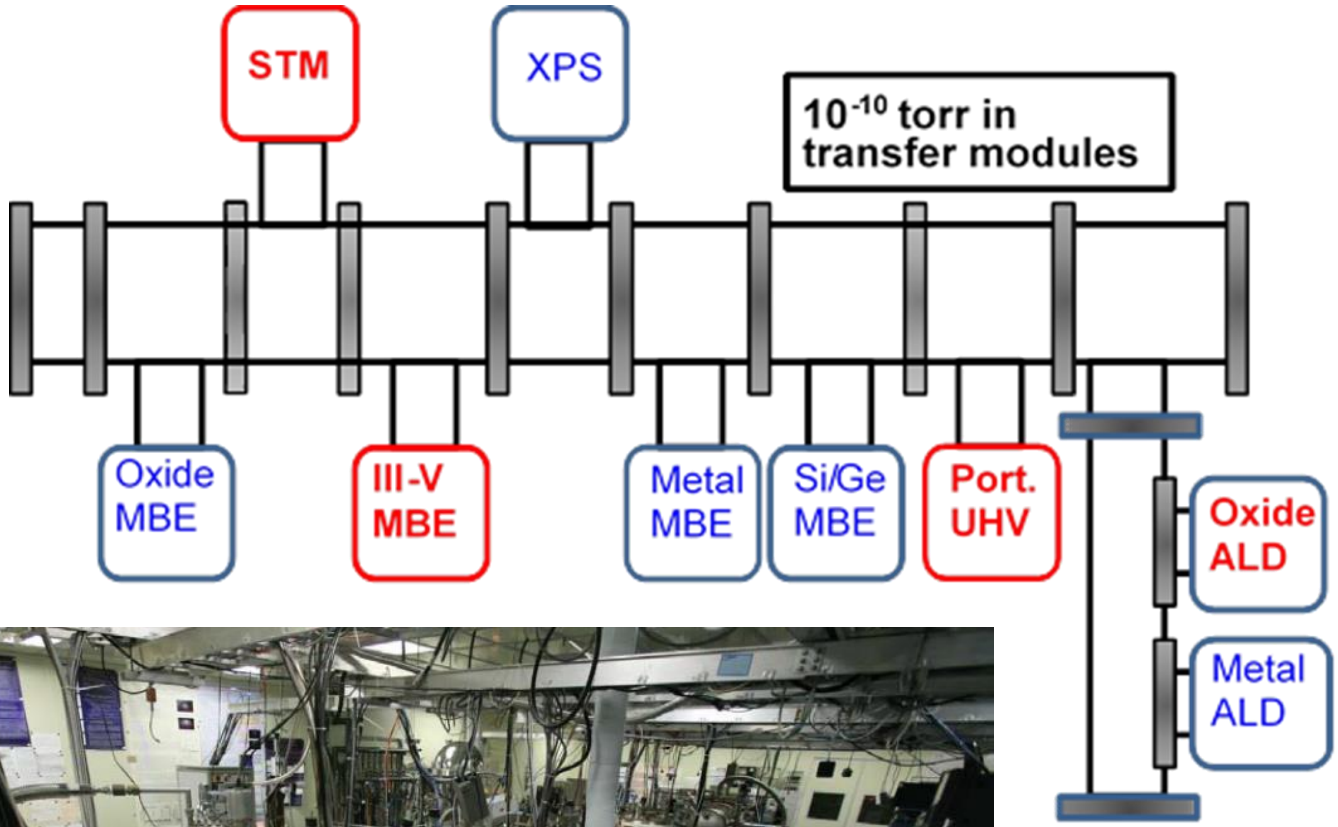


S. Takagi and M. Takenaka, ECS (2011)

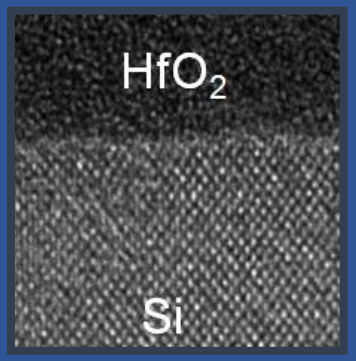
High dielectric constant oxides

Dielectrics	SiO_2	Al_2O_3	HfO_2	Gd_2O_3	Y_2O_3	La_2O_3
Dielectric constant	3.9	9	20	14	15-24	30
Band gap (eV)	8.9	8.7	5.7	5.8	5.8	4.3
Conduction band offset to GaAs (eV)	3.3	3.2	1.51	1.55	2.2	2.4
Valence band offset to GaAs (eV)	4.2	4.1	2.79	2.85	2.1	0.5

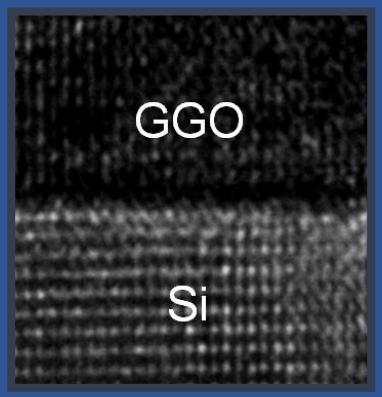
In-situ prepared oxide/semi. interfaces



Direct Deposition of High-κ Oxides *Interfacial layer free !!*



W. C. Lee, *et al.*, J. Cryst. Growth, 278, 619 (2005).



T. D. Lin, *et al.*, J. Cryst. Growth, 301, 386 (2007).

ALD- and MBD-Y_2O_3 on (In)GaAs

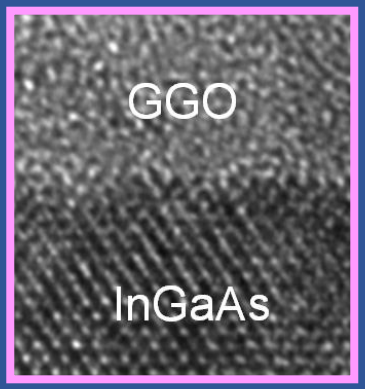
S. Y. Wu, *et al*, MEE 147, 310 (2015), and P. Chang et al, Appl. Phys. Express 4 114202 (2011).

M. Hong, *et al.*, J. Vac. Sci. Technol. B 14(3), 2297 (1996), and Appl. Phys. Lett. 76, 312 (2000).

ALD- and MBD-HfO_2 on (In)GaAs

T. D. Lin, *et al.*, Appl. Phys. Lett. 103, 253509 (2013).

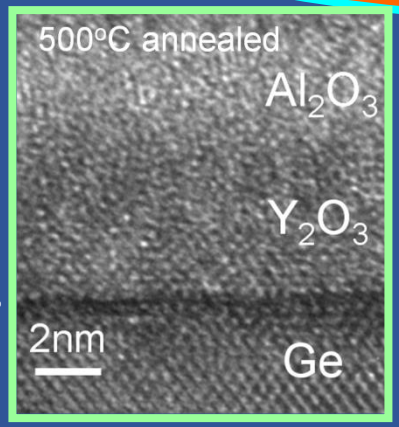
Molecular-beam-deposited and ALD oxides



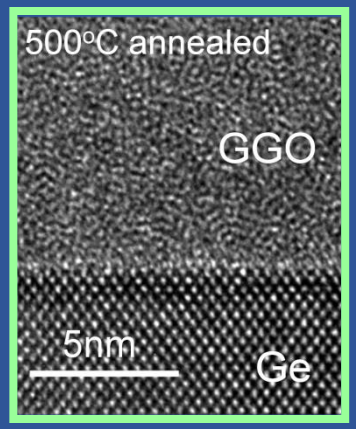
T. D. Lin, *et al.*, Appl. Phys. Lett. 93, 033516 (2008).

ALD- and MBD-Y_2O_3 on GaSb

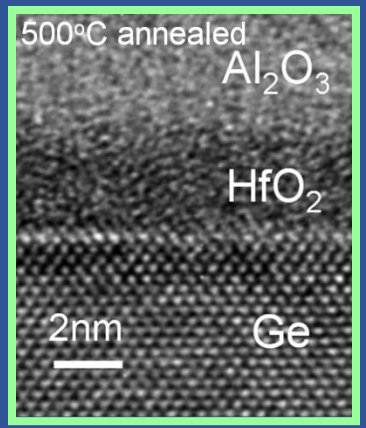
R. L. Chu, *et al.*, Appl. Phys. Lett. 105, 182106 (2014).



L. K. Chu, *et al.*, J. Cryst. Growth, 311, 2195 (2009).



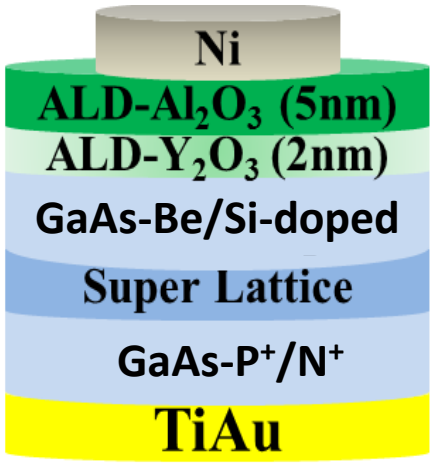
L. K. Chu, *et al.*, Appl. Phys. Lett. 94, 202108 (2009).



W. C. Lee, *et al.*, J. Cryst. Growth, 311, 2187 (2009).

GaAs MOS capacitor structure

Y_2O_3/GaAs

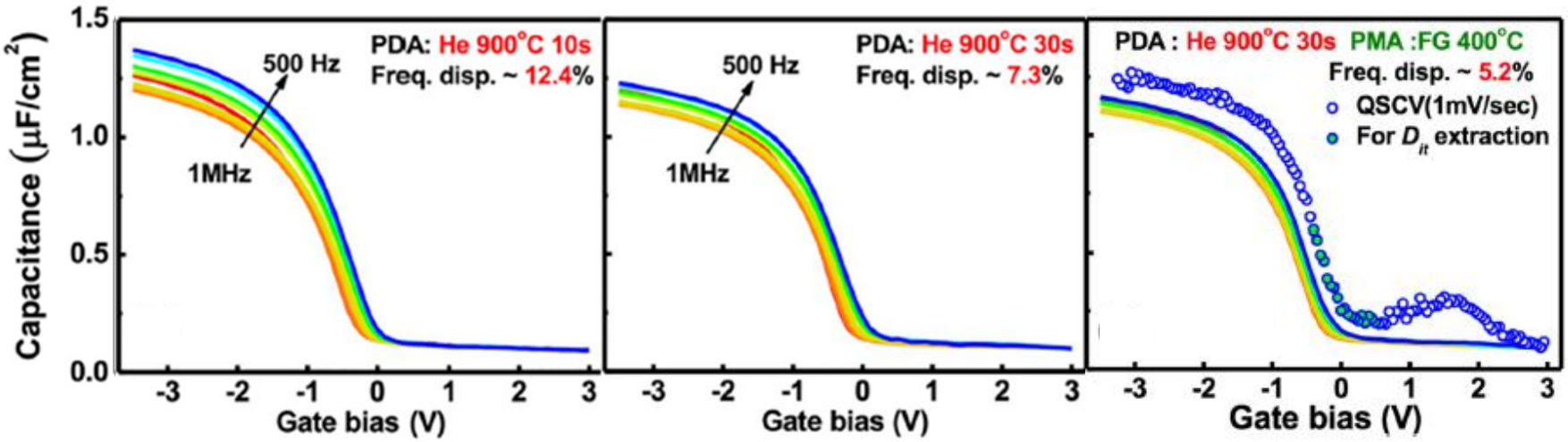


GaAs MOSCAPs process flow

- MBE prepared GaAs(001)-4×6 surface
- Deposition of ALD-Al_2O_3/Y_2O_3
- Post deposition annealing
  (900^oC 60s N_2 for Y_2O_3 samples)
- 100nm Ni metal gate formation
- Ti/Au as back contact electrodes

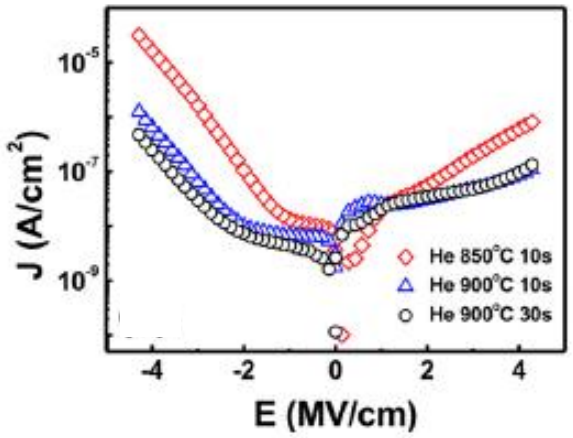
Amorphous MBE-HfO_2 for GaAs passivation

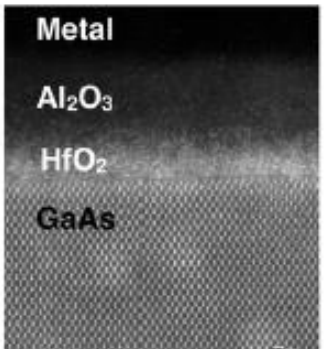
CV characteristics



- **Amorphous thin HfO_2** intended to prevent multi-domain HfO_2 crystal when annealed > 600°C
- **Thermal stability > 900°C**
- D_{it} < 1 x 10^{12} $eV^{-1}cm^{-2}$ **min. 1.3 x 10^{11} $eV^{-1}cm^{-2}$**

JE characteristics & STEM image



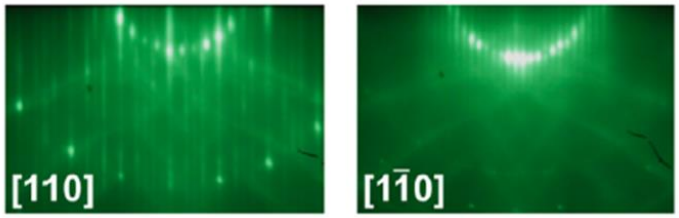


900°C-annealed sample

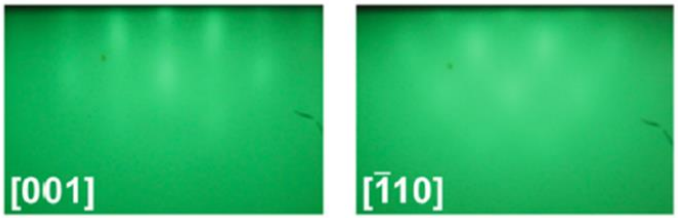
H. W. Wan, et al., MEE **178**, 154 (2017)

Single crystalline MBE-Y_2O_3 for GaAs passivation

RHEED: GaAs (001)-4x6



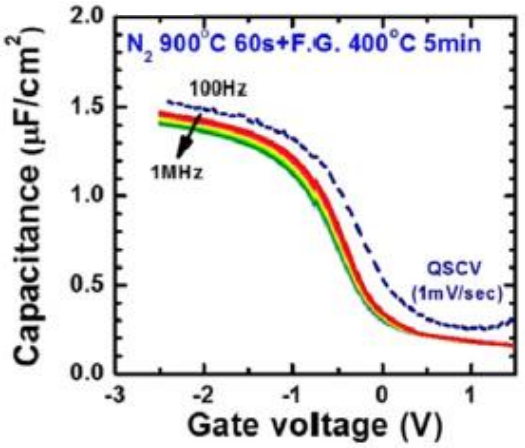
RHEED: MBE-Y_2O_3(110)

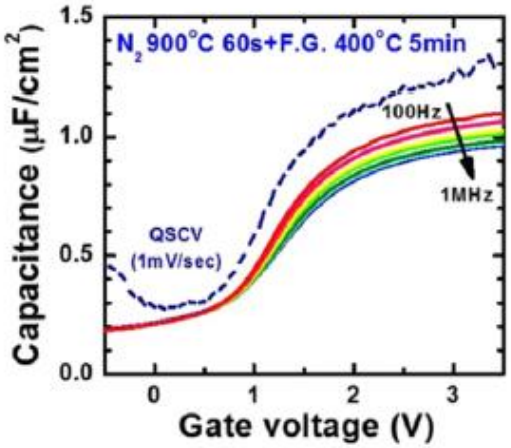


- **Single crystalline Y_2O_3(110) on GaAs(001) similar to structure of Gd_2O_3(110) on GaAs(001)**
- **Thermal stability > 900°C**
- **D_{it} ~(3-5) x 10^{11} $eV^{-1}cm^{-2}$**

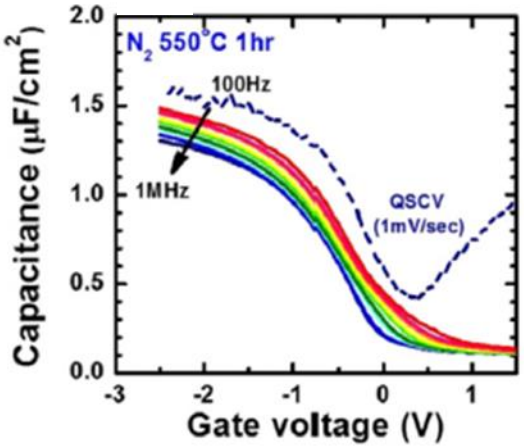
CV characteristics
– Comparison with ALD-Al_2O_3 passivation

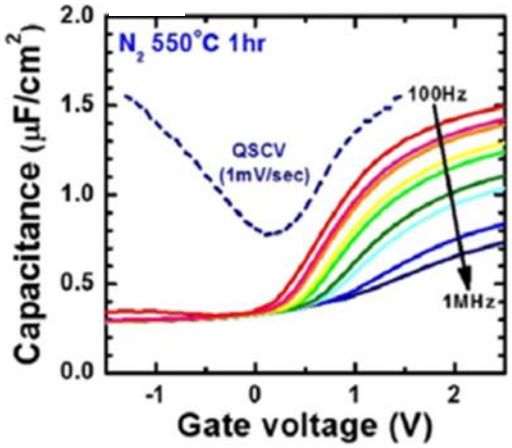
MBE-Y_2O_3 passivation





ALD-Al_2O_3 passivation



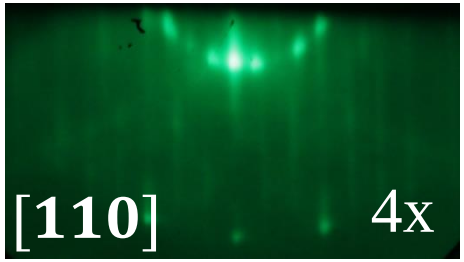


H. W. Wan, K. Y. Lin, et al., JCG **477**, 179 (2017)

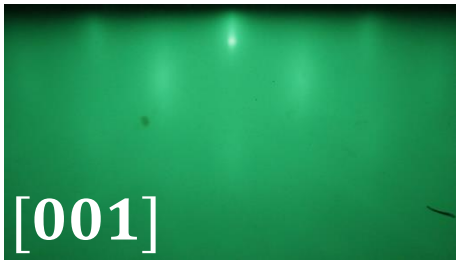
Single crystalline ALD-Y_2O_3 for GaAs passivation

RHEED:
ALD-Y_2O_3(110) on GaAs (001)-4x6

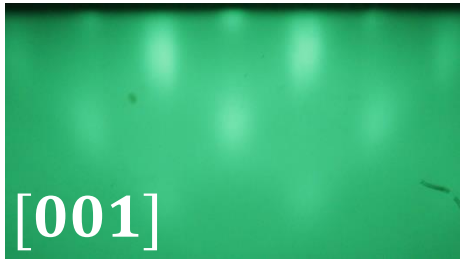
GaAs(001) surface



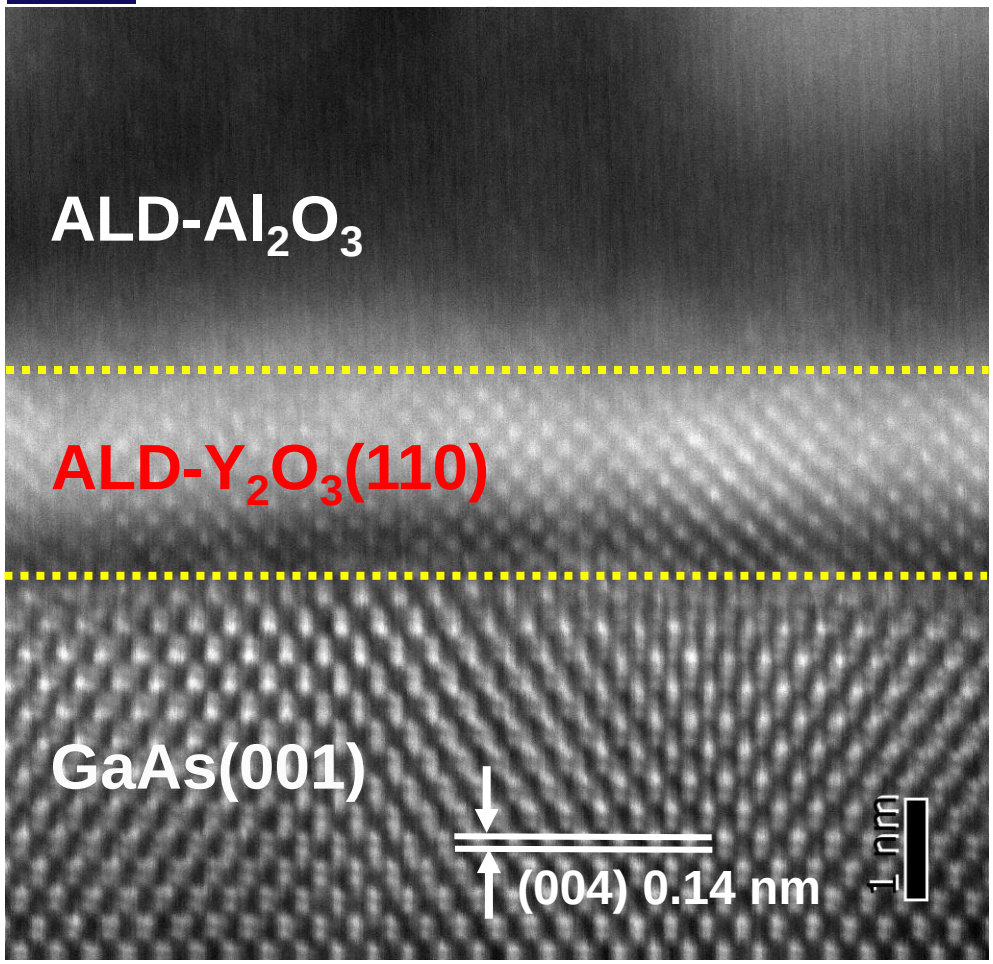
Y_2O_3(110) 1.0 nm



Y_2O_3(110) 2.3 nm



TEM



S. Y. Wu, M. Hong, et al, *Microelectron. Eng.* **147**, 310-313 (2015)
K. Y. Lin, L. B. Young, M. Hong, et al, *Microelectron. Eng.* **178**, 271-274 (2017)

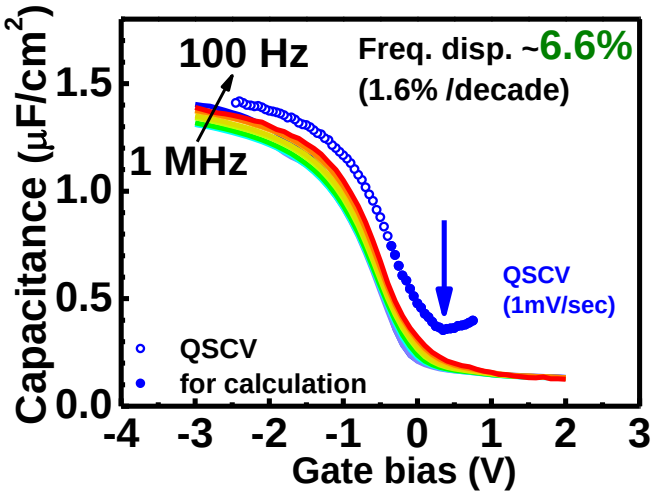
Single crystalline ALD-Y_2O_3 for GaAs passivation

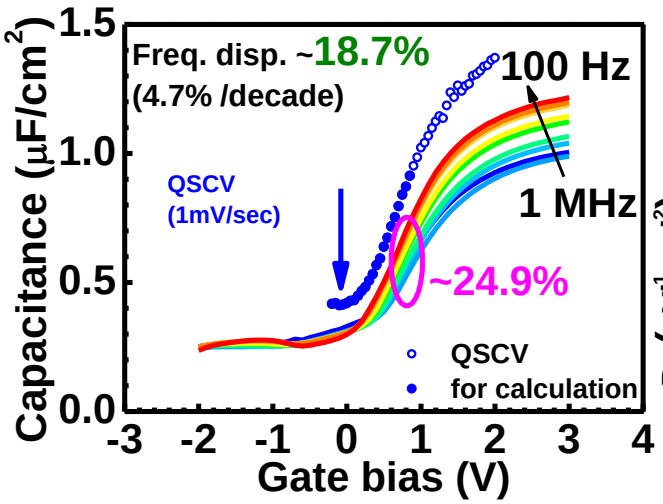
CV characteristics

In-situ MBE + ALD

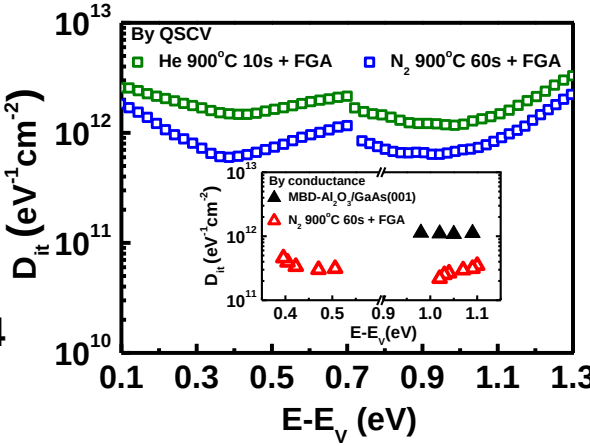
Y. C. Chang, M. Hong, et al, APL **97**, 112901 (2010)
Y. H. Lin, M. Hong, et al, APEX **9**, 081501 (2016)
T. W. Chang, M. Hong, et al, unpublished (2017)

He 900°C 10s + FGA

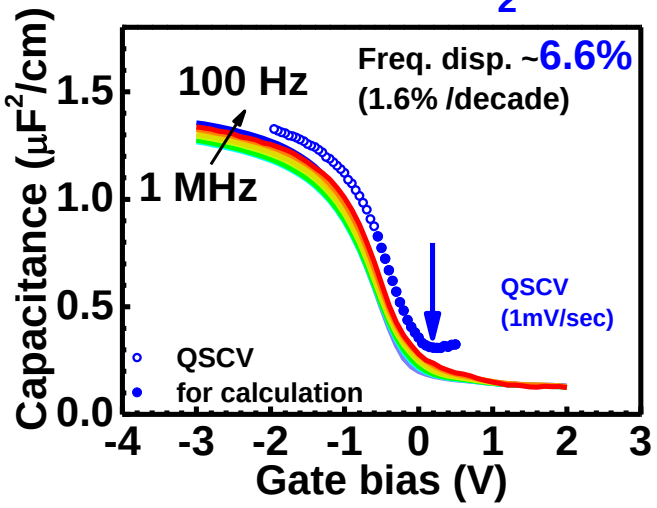


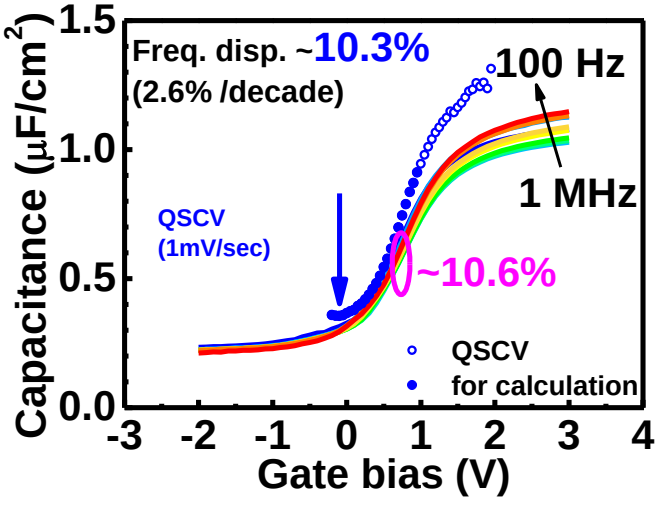


D_{it} distribution



N_2 900°C 60s + FGA





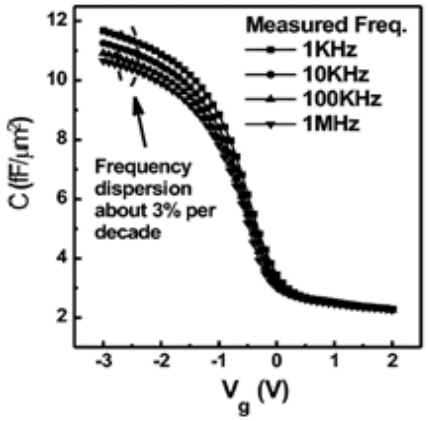
- Single crystalline Y_2O_3 on GaAs
- Thermal stability > 900°C
- D_{it} ~(2-3) x 10^{11} $eV^{-1}cm^{-2}$
- No mid-gap peak

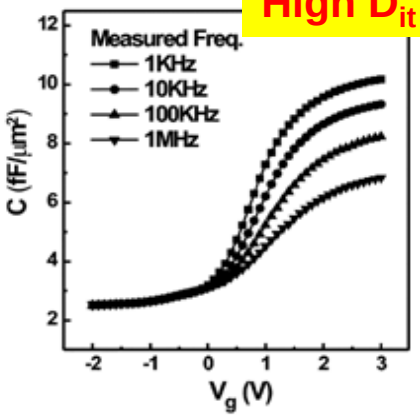
Ex-situ and in-situ ALD-Al_2O_3 for GaAs passivation

ALD-HfO_2/Al_2O_3/GaAs(001) with NH_4OH surface pretreatment

T. Yang, P. D. Ye, R. M. Wallace et al., *Appl. Phys. Lett.*, **91**, 142122 (2007)

High D_{it}

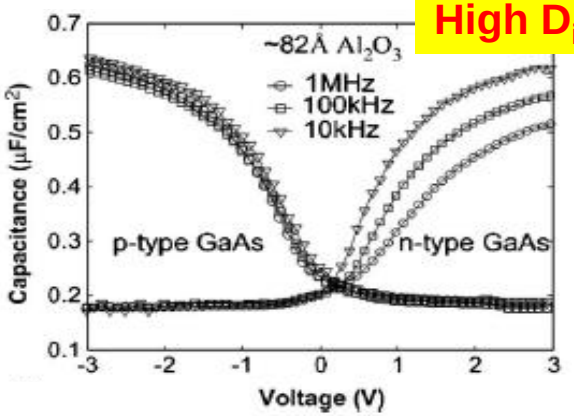




ALD-Al_2O_3/GaAs(001) with $(NH_4)_2S$ surface pretreatment

D. Shahrjerdi, et al. *Appl. Phys. Lett.*, **92**, 203505 (2008)

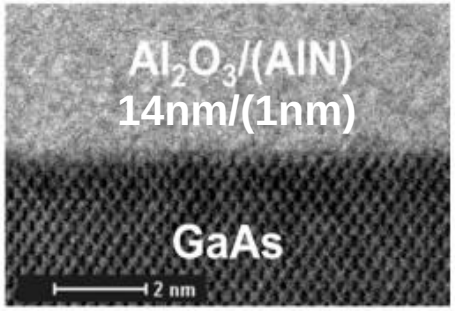
High D_{it}

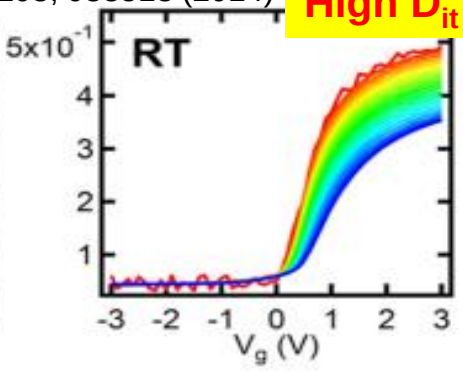


ALD-Al_2O_3/n-GaAs(001) with AlN interfacial passivation layer

T. Aoki et al., *Appl. Phys. Lett.*, **105**, 033513 (2014)

High D_{it}

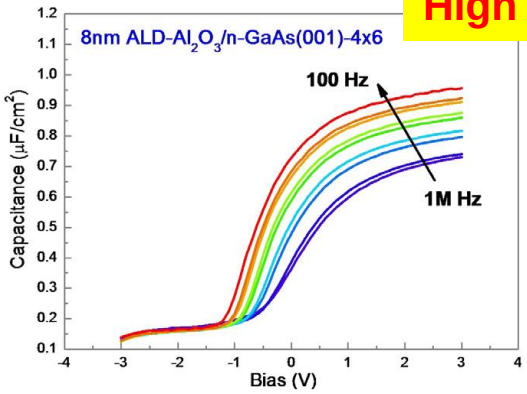




ALD-Al_2O_3/n-GaAs(001) without surface pretreatments

Y. H. Chang, M. Hong et al., *Microelectron. Eng.*, **88**, 1101-1104 (2011)

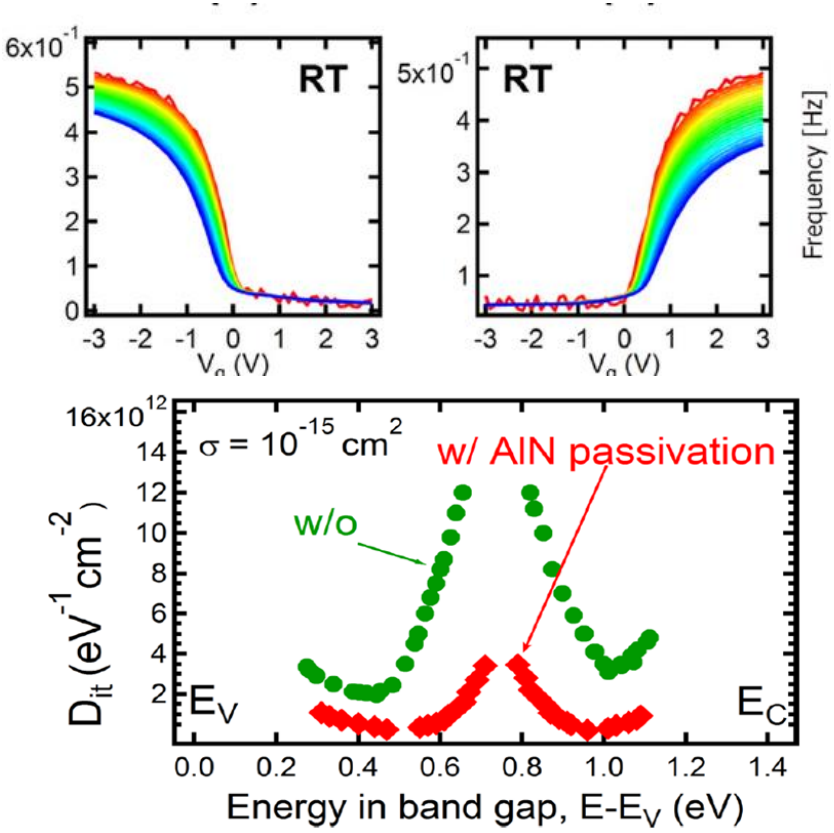
High D_{it}



Ex-situ ALD-Al_2O_3 for GaAs passivation

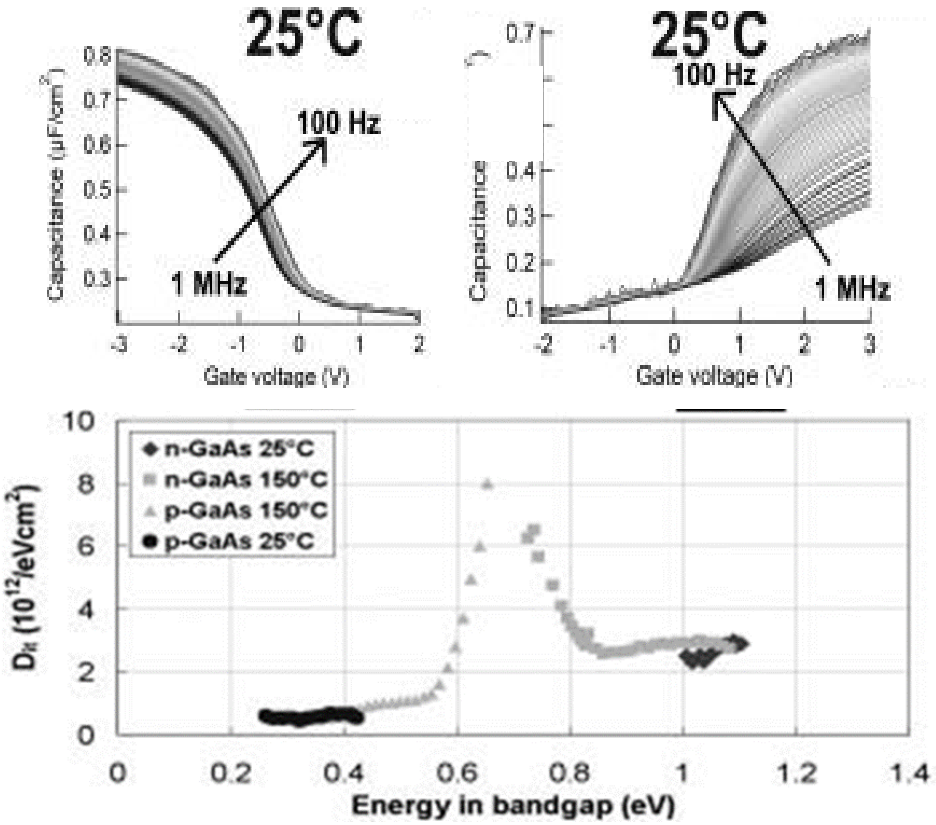
ALD-Al_2O_3/GaAs(001) with AlN interfacial passivation layer

T. Aoki, et al. Appl. Phys. Lett. **105**, 033513 (2014)



ALD-Al_2O_3/GaAs(001) with $(NH_4)_2S$ surface pretreatment

G. Brammertz *et al.* Appl. Phys. Lett. **93**, 183504 (2008)



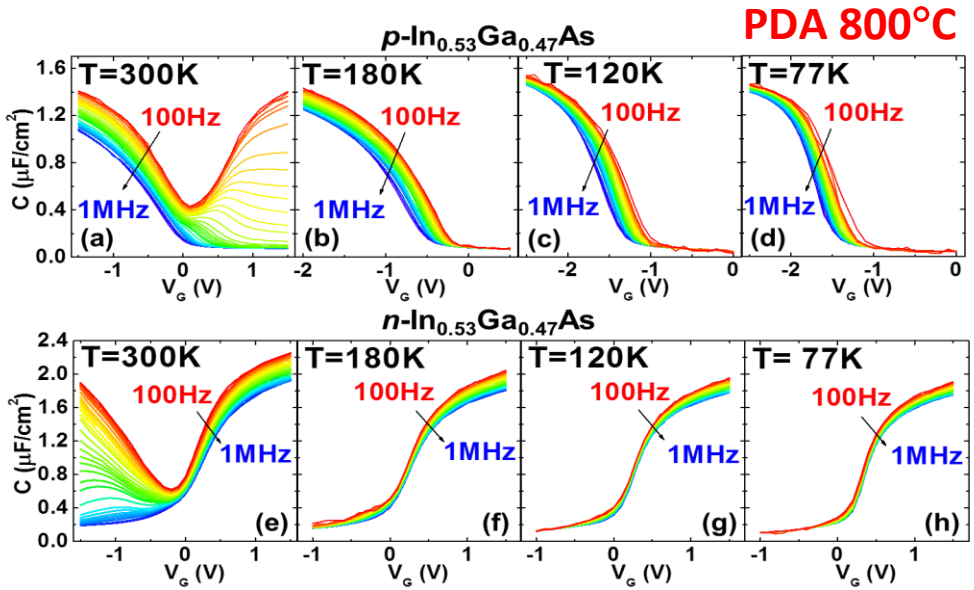
The D_{it} spectrum shows a midgap peak!

Ultimate CMOS – ALD-HfO_2/MBE-$In_{0.53}Ga_{0.47}As$

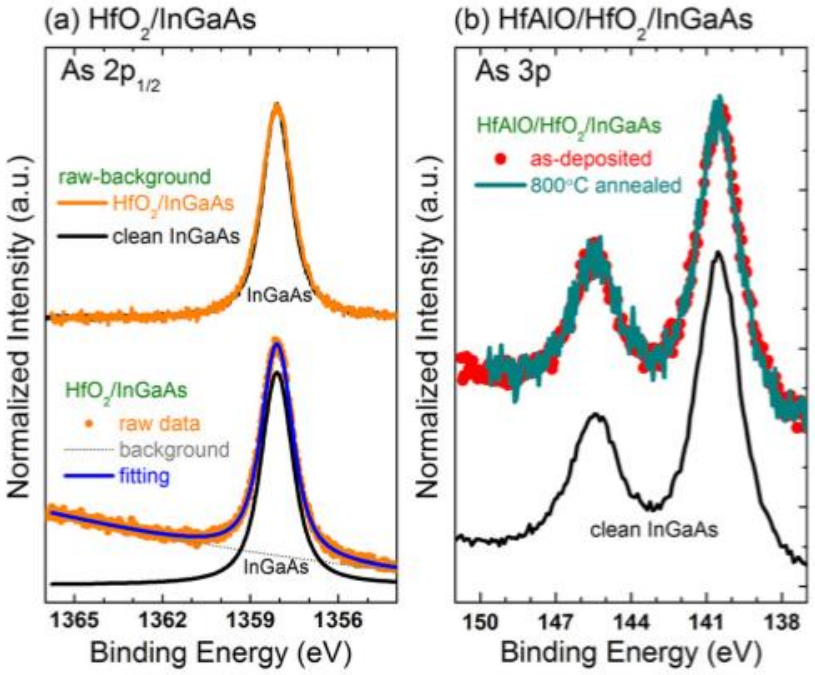
T. D. Lin, et al. APL **100**, 172110 (2012)

CV characteristics

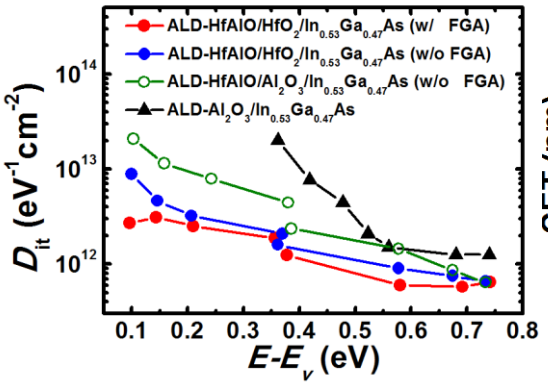
HfAlO/HfO_2 (0.8nm)/$In_{0.53}Ga_{0.47}As$



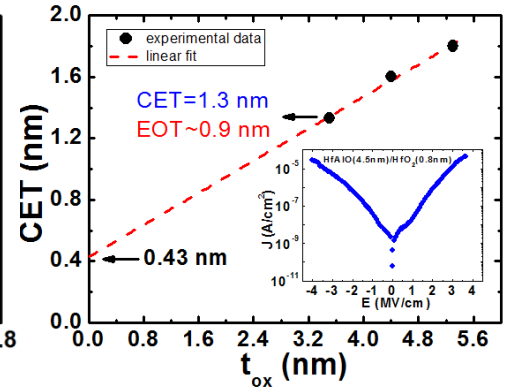
XPS



D_{it} distribution



CET projection

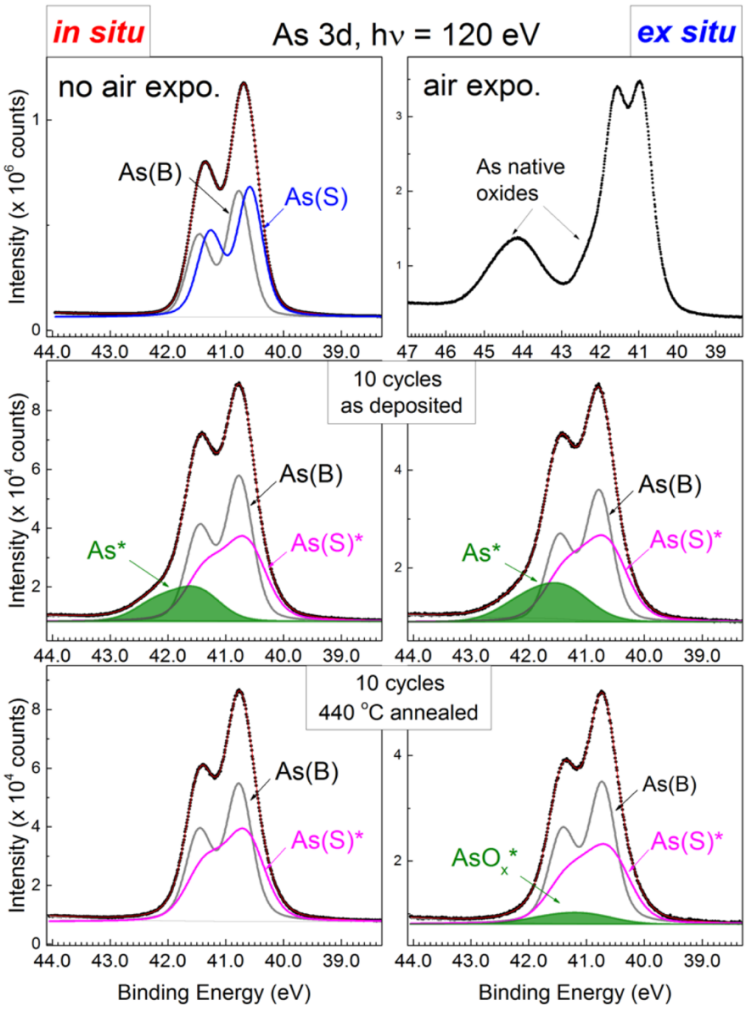


- **Tetra-valence** oxide HfO_2 do passivate $In_{0.53}Ga_{0.47}As$
- Thermal stability **> 800°C**
- D_{it} **~(6-20) x 10^{11} $eV^{-1}cm^{-2}$ without mid-gap peak**
- **EOT ~0.9 nm** achieved

Ultimate CMOS – ALD-Al_2O_3/MBE-$In_{0.53}Ga_{0.47}As$

M. Hong, et al., APL **111**, 123502 (2017)

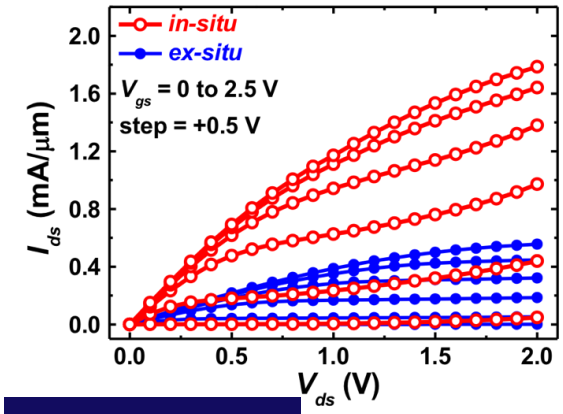
HR-SRPES

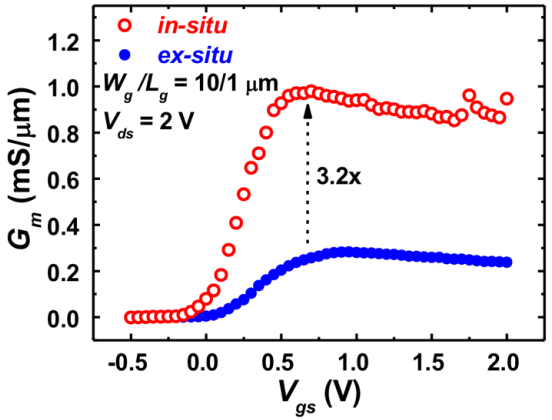


AsO_x-free interface

AsO_x remained

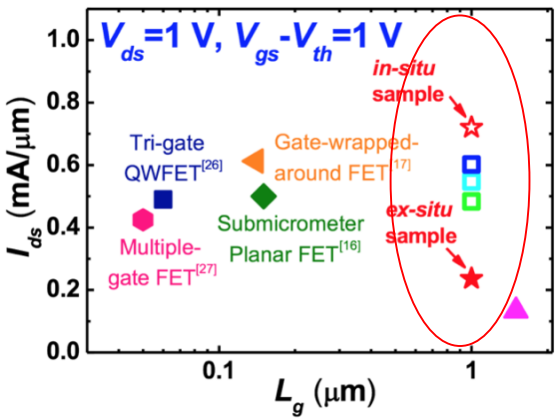
Self-aligned inversion-channel device

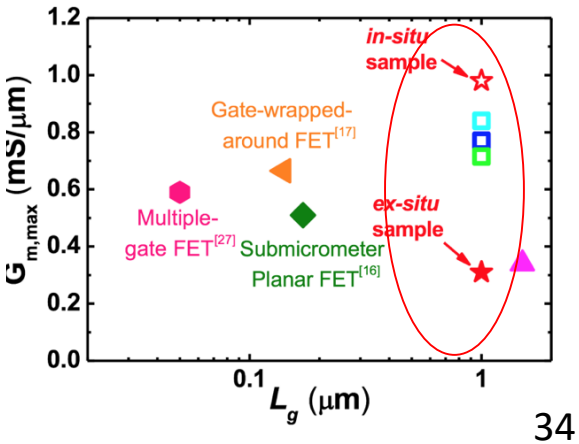




Benchmark

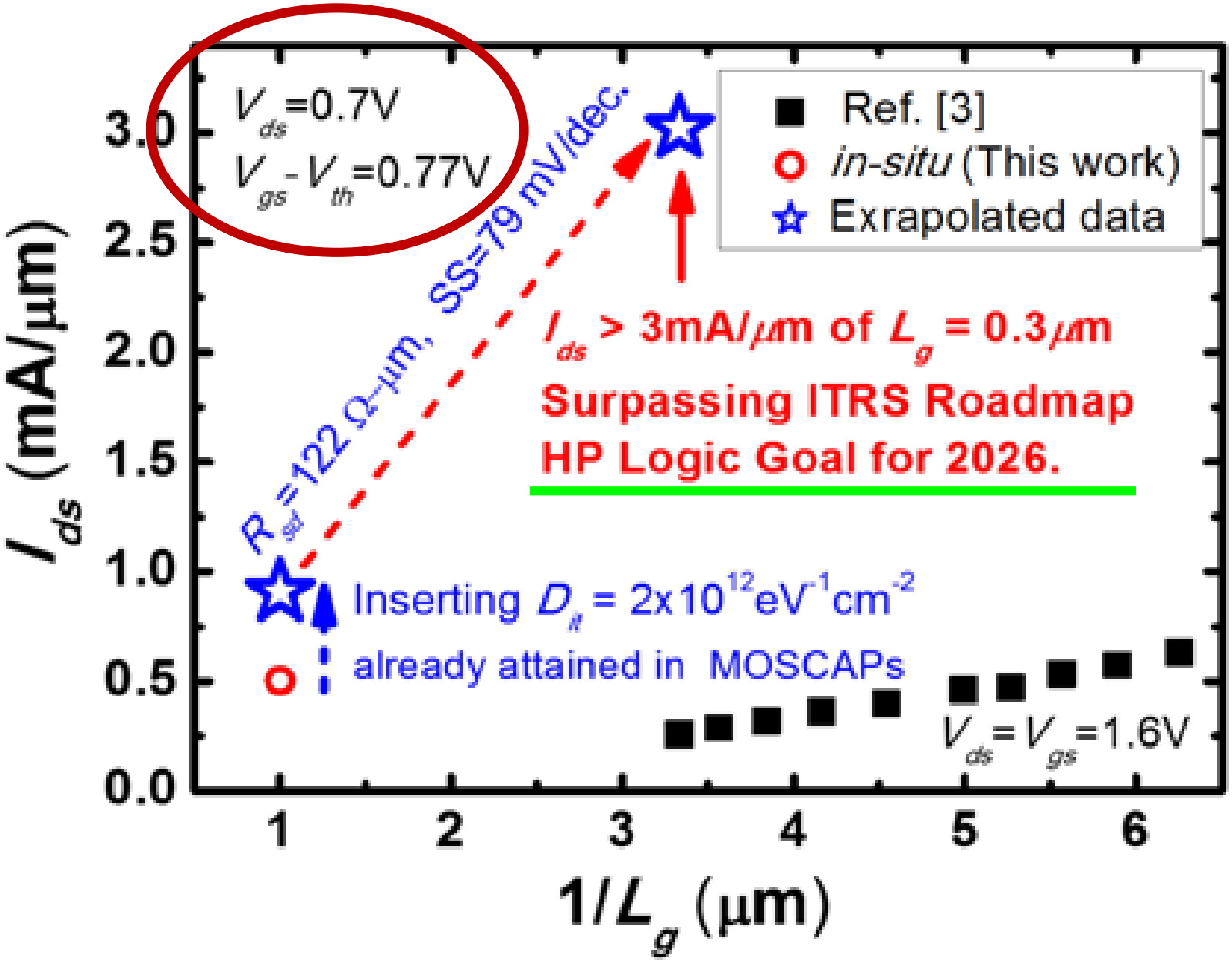
- This Work (*in-situ* ALD-Al_2O_3/InGaAs)
- NTU/NTHU (ALD-HfO_2/InGaAs)[20]
- NTU/NTHU (MBE-Y_2O_3/InGaAs)[19]
- NTHU (MBE-GGO/InGaAs)[18]
- This Work (*ex-situ* ALD-Al_2O_3/InGaAs)
- Intel (High-k/InGaAs)[26]
- IMEC (ALD-Al_2O_3/InGaAs)[25]
- University of Texas at Austin (ALD-Al_2O_3/InGaAs)[17]
- Purdue University (ALD-Al_2O_3/InGaAs)[16]
- National University of Singapore (ALD-Al_2O_3/InGaAs)[27]





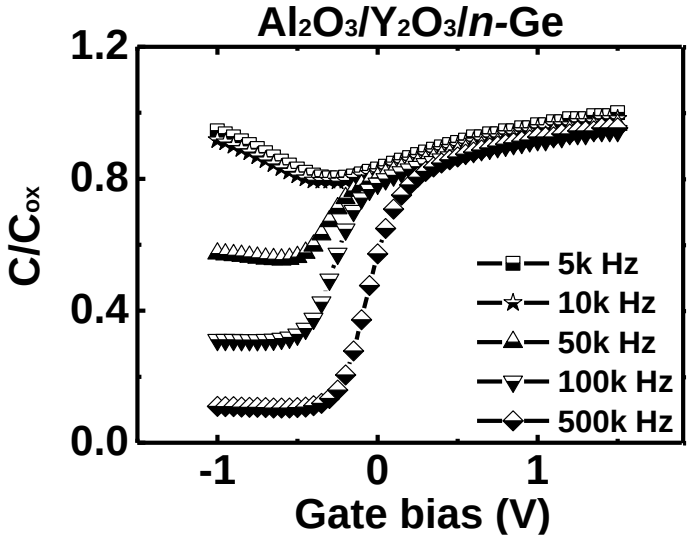
Ultimate CMOS – ALD-Al_2O_3/MBE-$In_{0.53}Ga_{0.47}As$

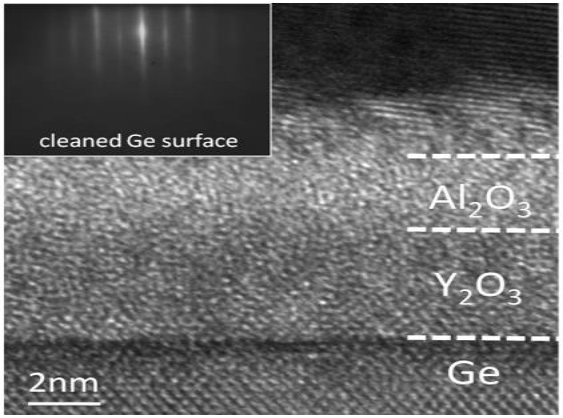
M. Hong, et al., APL **111**, 123502 (2017)

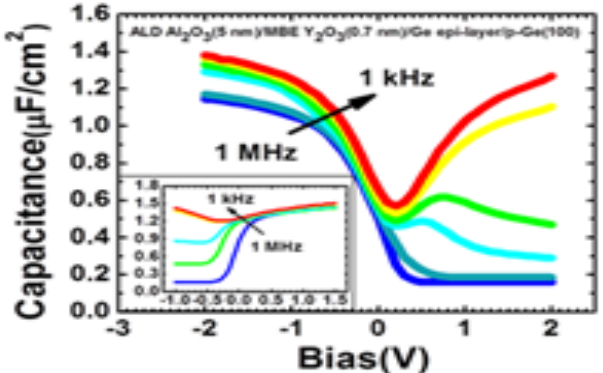


Common gate MBE-Y_2O_3 for Ge passivation

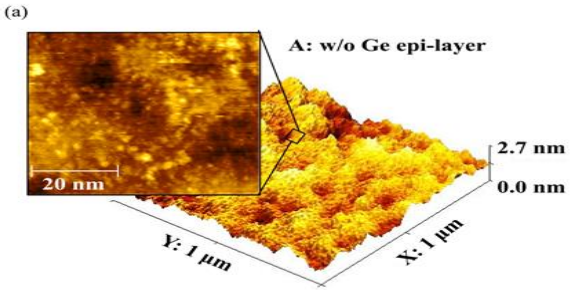
Ge

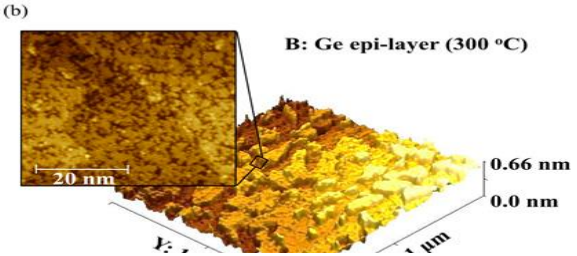




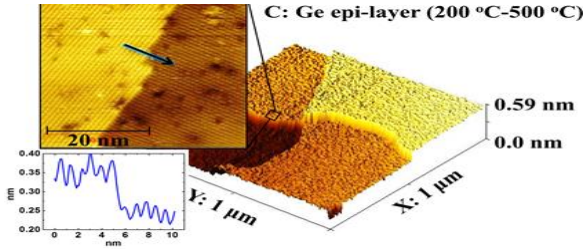


Root mean square surface roughness (R_q) is around 3.5 Å in a 1x1 μm² area.





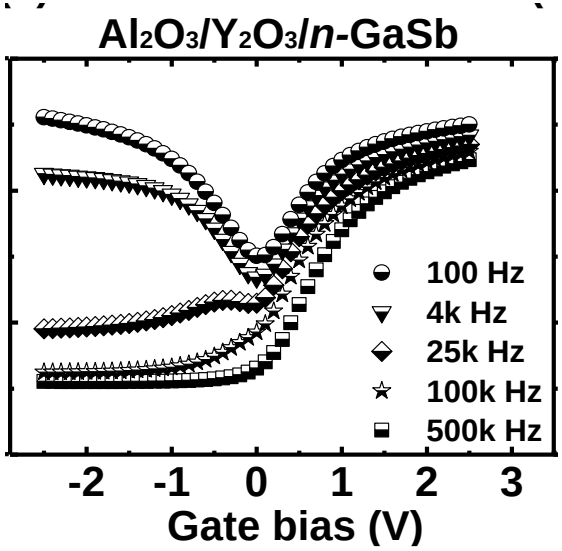
Root mean square surface roughness (R_q) is around 1 Å in a 1x1 μm² area.

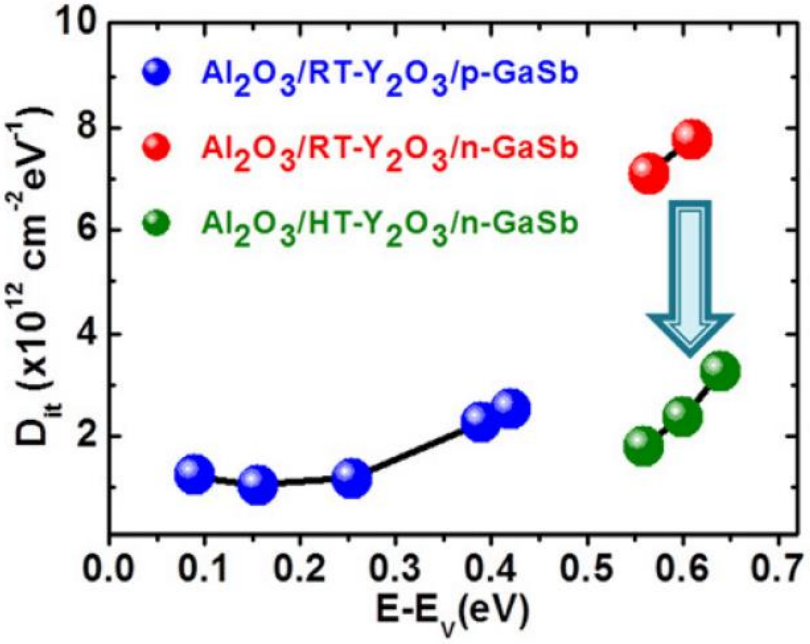


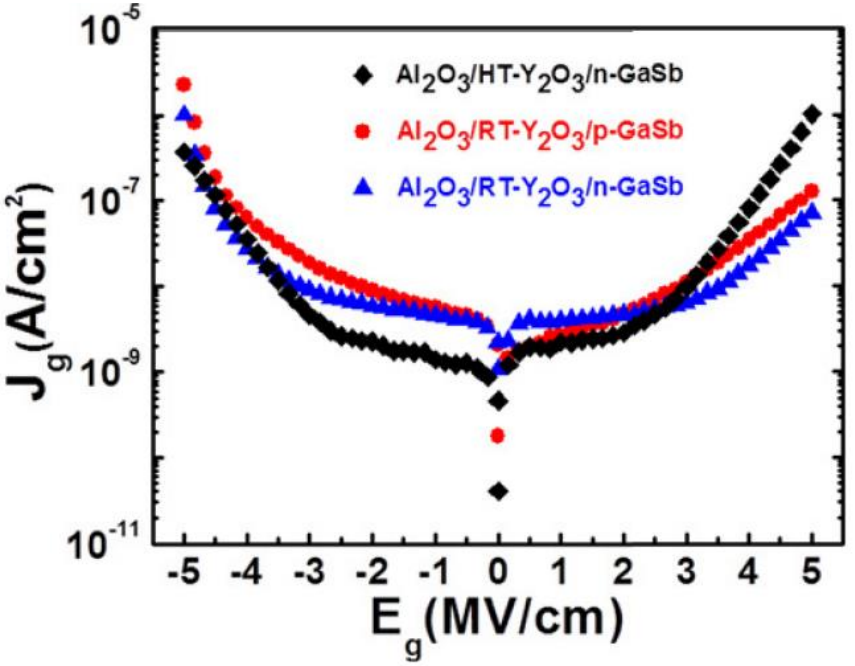
L.K. Chu et al., J. Crystal Growth 311, 2195 (2009)
R.L. Chu et al., Appl. Phys. Lett. 104, 202102 (2014)

Common gate MBE-Y_2O_3 for GaSb passivation

GaSb



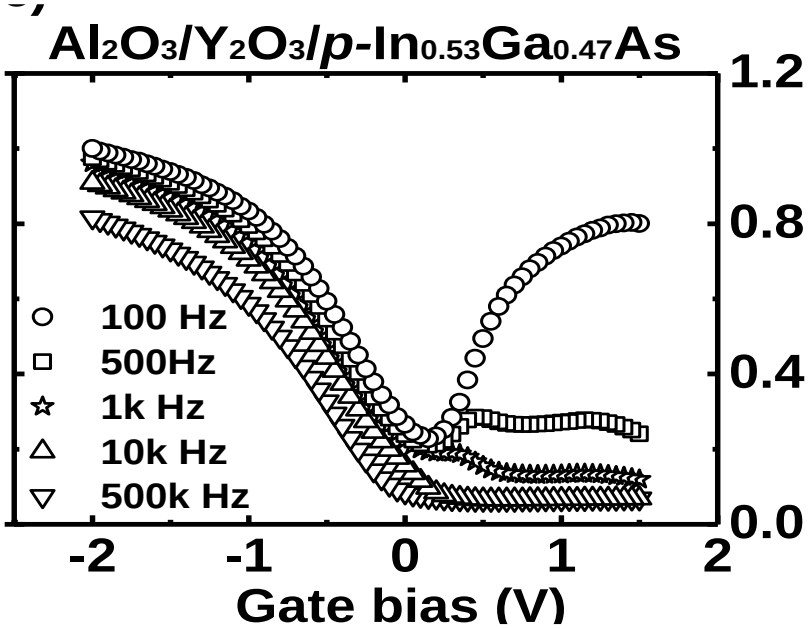


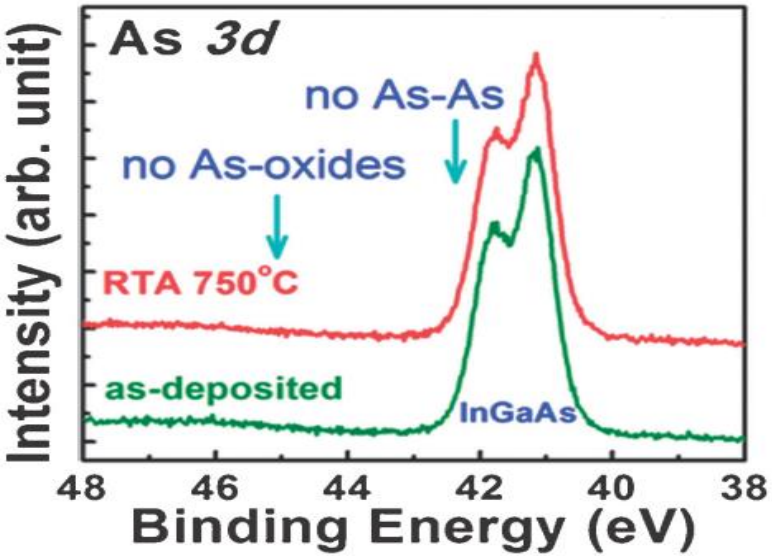


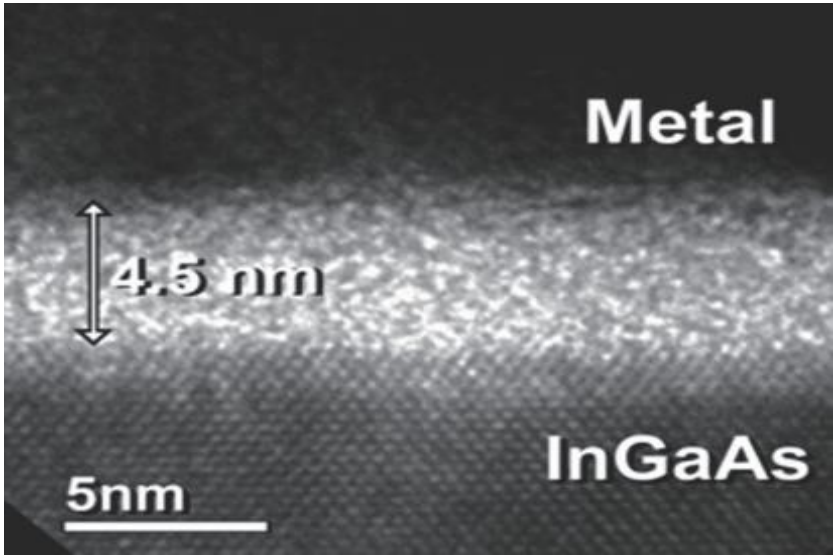
R.L. Chu et al., Appl. Phys. Lett. 104, 202102 (2014)
R.L. Chu et al., Appl. Phys. Lett. 105, 182106 (2014)

Common gate MBE-Y_2O_3 for InGaAs passivation

(In)GaAs

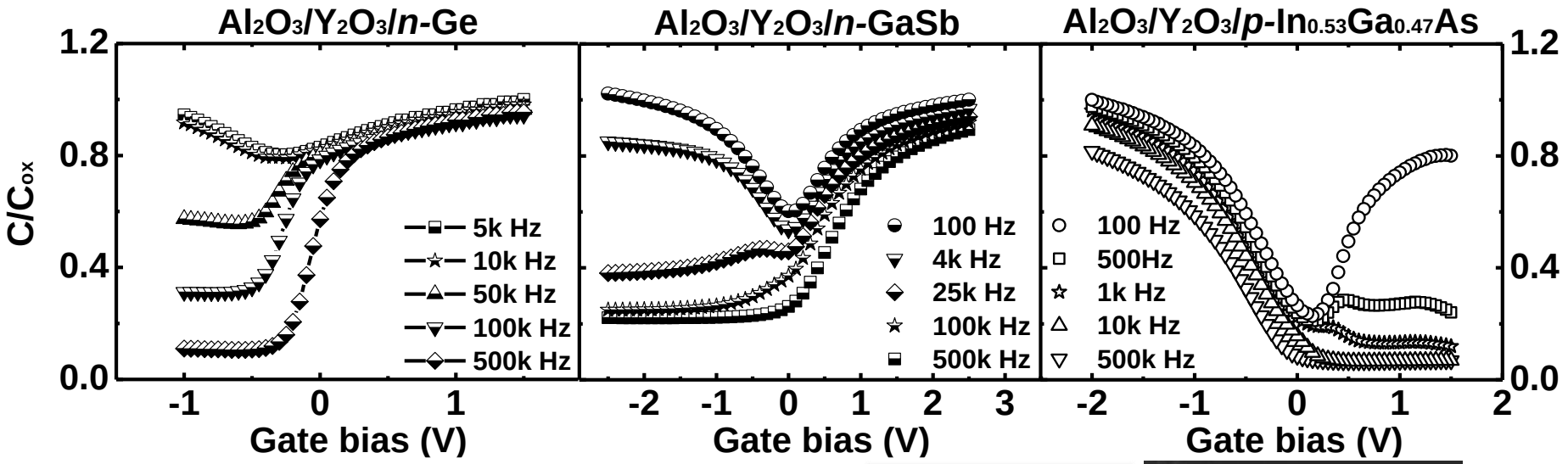


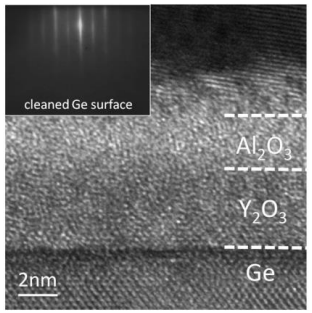




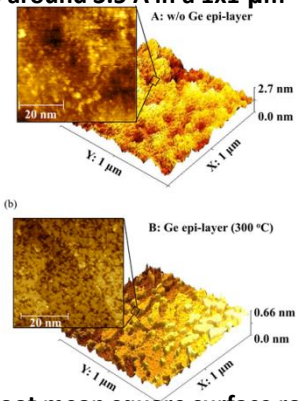
P. Chang et al., Appl. Phys. Express 4, 114202 (2011)

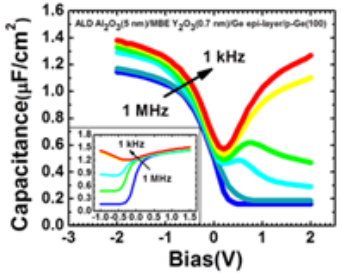
Common gate MBE-Y_2O_3 for semiconductors



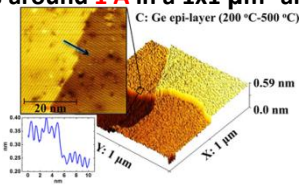


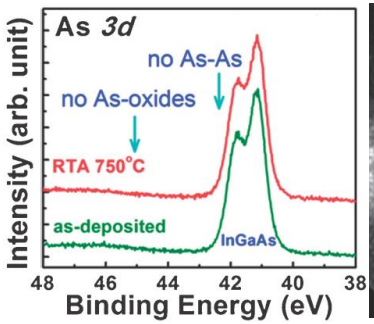
Root mean square surface roughness (R_q) is around 3.5 Å in a 1x1 μm² area.

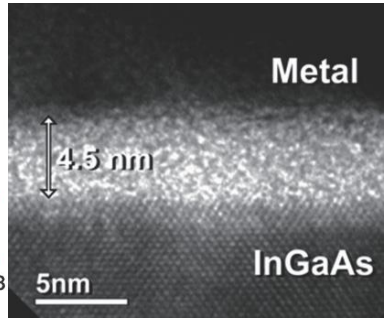


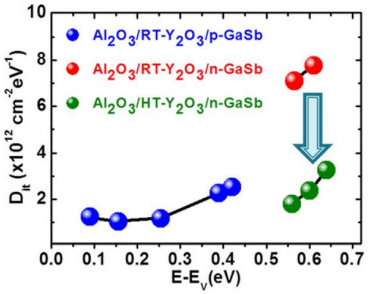


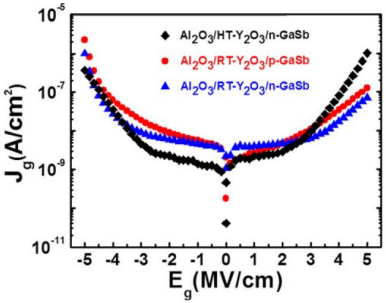
Root mean square surface roughness (R_q) is around 1 Å in a 1x1 μm² area.











L.K. Chu et al., J. Crystal Growth 311, 2195 (2009)
R.L. Chu et al., Appl. Phys. Lett. 104, 202102 (2014)
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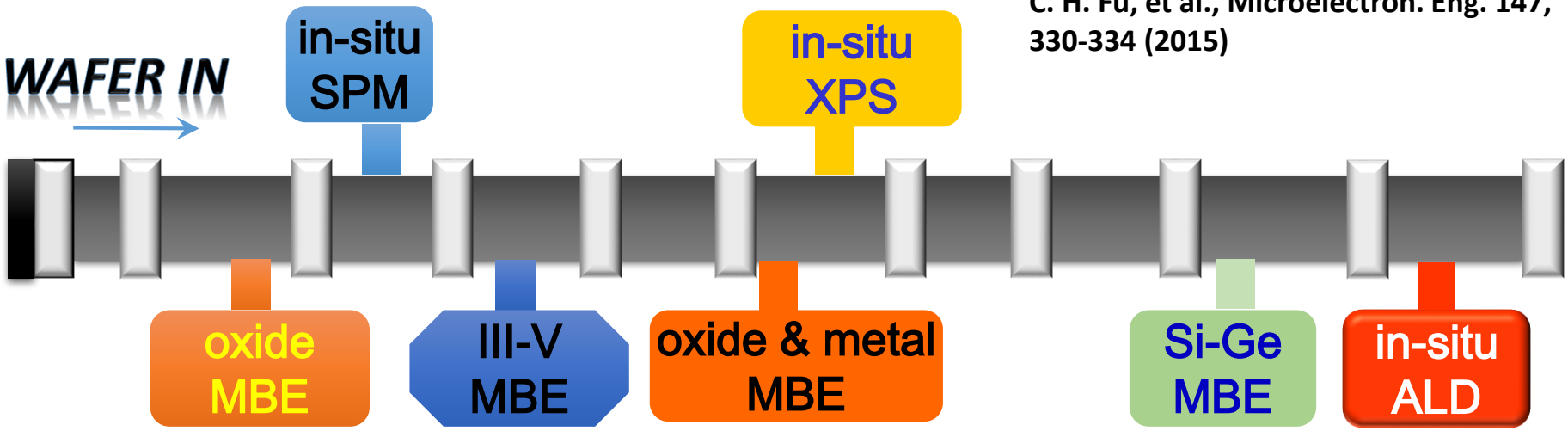
P. Chang et al., Appl. Phys. Express 4, 114202 (2011)

Fabrication process for E-mode MOSFETs

C. H. Fu, et al., Microelectron. Eng. 147, 330-334 (2015)



Process flow for Self-aligned MOSFET

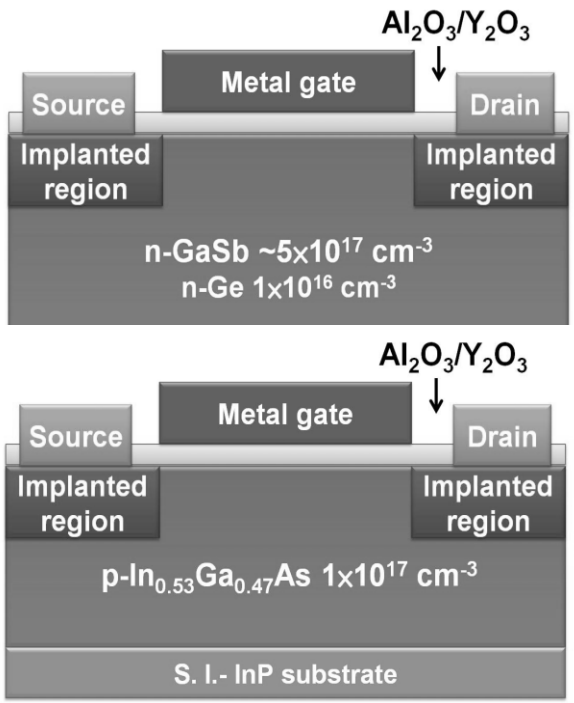
$In_{0.53}Ga_{0.47}As$	GaSb	Ge
Growth of $In_{0.53}Ga_{0.47}As$ layer	De-capping of arsenic-capped GaSb substrate	UHV annealing to ~450°C to remove Ge native oxide

Direct deposition of MBE-Al_2O_3/Y_2O_3 as gate dielectric

metal gate patterning and formation

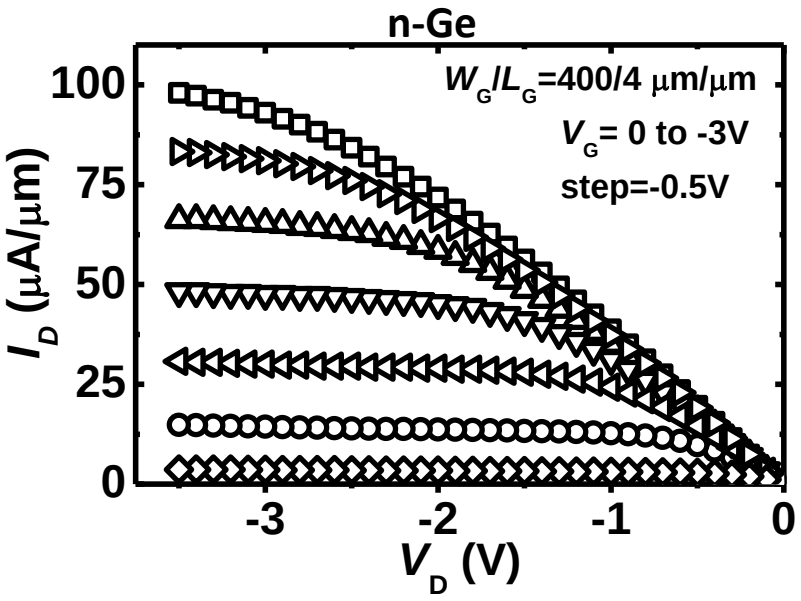
S/D region patterning and ion implantation

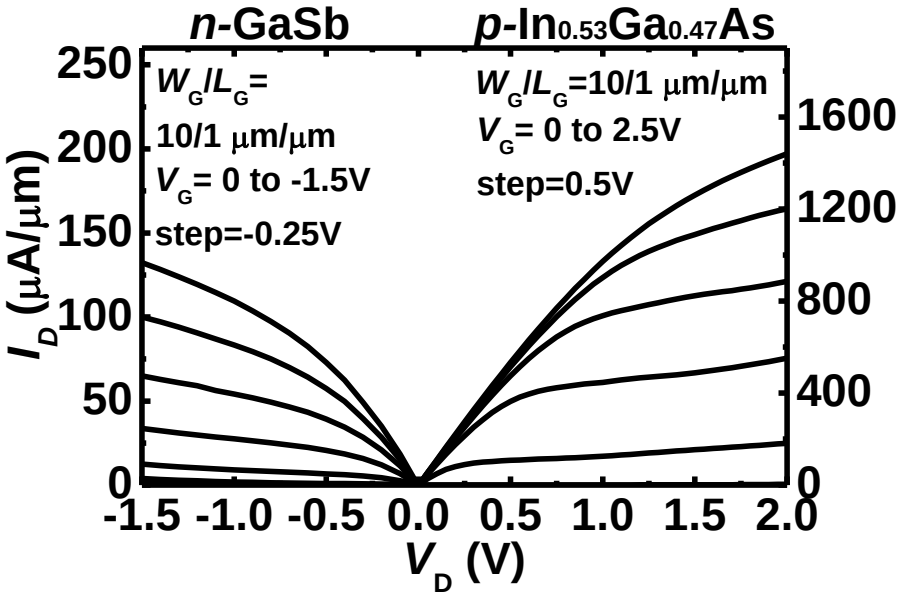
S/D activation: RTA at 750°C in N_2 for 10s	**S/D activation:** RTA at 500°C in N_2 for 30s	**S/D activation:** RTA at 500°C in N_2 for 10min
S/D metallization: Pd/Ge/Ti/Pt	**S/D metallization:** Ni	**S/D metallization:** Ti/Al



Electrical characteristics of MOSFETs

C. H. Fu, et al., Microelectron. Eng. 147, 330-334 (2015)





n-Ge

- W/L= 400/4 μm/μm
- $I_{D,max}$= 98 mA/mm @V_G= -3V, V_D= -3.5V
- $G_{m,max}$~ 42 mS/mm @ V_D= -3.5V
- μ_{FE}= 241 cm²/V·s

n-GaSb

- W/L= 10/1 μm/μm
- $I_{D,max}$= 130 mA/mm @V_G= -1.5V, V_D= -1.5V
- $G_{m,max}$~ 90 mS/mm @ V_D= -1.5V
- μ_{FE}= 200 cm²/V·s

p-$In_{0.53}Ga_{0.47}As$

- W/L= 10/1 μm/μm
- $I_{D,max}$= 1440 mA/mm @V_G= 2.5V, V_D= 2V
- $G_{m,max}$~ 770 mS/mm @ V_D= 2.5V
- μ_{FE}= 2100 cm²/V·s

Electrical characteristics of MOSFETs

$In_{0.53}Ga_{0.47}As$ inversion channel nMOSFET

Dielectrics	L_G (μm)	$I_{d,max}$ (μA/μm)	$I_d \times L_G$ (μA)	$G_{m,max}$ (μS/μm)	$G_m \times L_G$ (μS)	S.S. (mV/dec.)	I_{on}/I_{off}	μ_{FE} (cm^2/Vs)[a]	
ALD-Al_2O_3	0.5	430	215	160	80	240	4×10^3	1200	Purdue U
UHV Al_2O_3/GGO	1	1050	1050	714	714	-	-	1300	
MOCVD HfAlO	0.25	420	105	45.3	11.3	200	-	-	NUS
ALD-Al_2O_3	0.6	678	406	354	212	194	-	-	
ALD-Al_2O_3/ HfO_2	1	1500	1500	840	840	103	10^4	1100	
Not listed	0.03	~1200	36	2230	66.9	-	~10^4	1000	**IBM**
Al_2O_3/Y_2O_3	1	1440	1440	770	770	97	10^4	2100	This work

Ge inversion channel pMOSFET

HfO_2/SiON/GeON	5	30	150	-	-	102	10^3	~300	NUS
$HfO_2/Si(SiO_2)$	0.125	1360	170	-	-	100	10^5	358	**Leuven**
SiO or Al_2O_3/GeO_2	200	0.4	80	-	-	120	-	400	Tokyo U
HfO_2/GeO_2	10	37.8	378	-	-	85	10^3	396	NUS
GGO	1	496	496	178	178	-	-	389	
Al_2O_3/GeO_x	50	1.5	75	-	-	-	~10^2	526	Tokyo U
Al_2O_3/Y_2O_3	4	98	392	43	172	-	5×10^2	241	This work

C. H. Fu, et al., Microelectron. Eng. 147, 330-334 (2015)

GaSb inversion channel pMOSFET

Al_2O_3	5	~0.6	3	-	-	250	100	~270	Stanford U
Al_2O_3	6	4	24	-	-	250	10^3	160	CAS Beijing
Al_2O_3	2	10	20	-	-	400	~10	25	Tokyo U/NTT
Al_2O_3/Y_2O_3	1	130	130	90	90	147	10^3	200	This work

Thank you for your attention!